

MS-7245 (Babel)

Version 0A

System Chipset:

Intel Broadwater - GMCH (North Bridge)

Intel ICH8(DO) (South Bridge)

On Board Chipset:

BIOS -- SPI Flash 8Mb or 16Mb

HD AUDIO -- ALC262

LPC Super I/O -- SMSC--SHC5017

LAN -- Intel Neneveh 82566

IDE-- VIA VT-6410

CLOCK -- ICSLP505-1

Main Memory:

2 CHANNEL DDR II * 4 (Max 8GB)

Expansion Slots:

PCIE x16 SLOT * 1

PCIE x1 SLOT * 1

PCI SLOT * 1

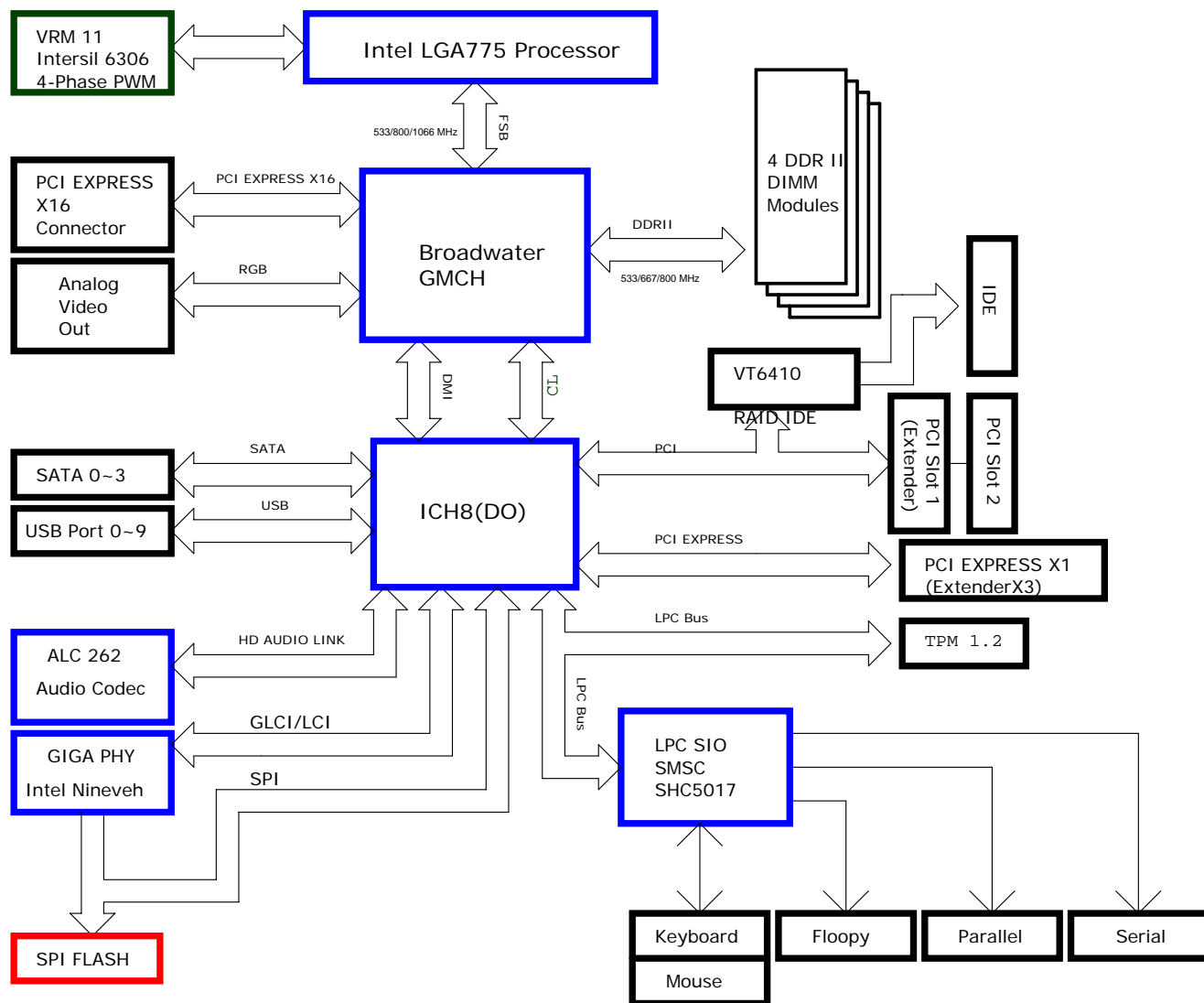
PCI Extender SLOT * 1

Intersil PWM:

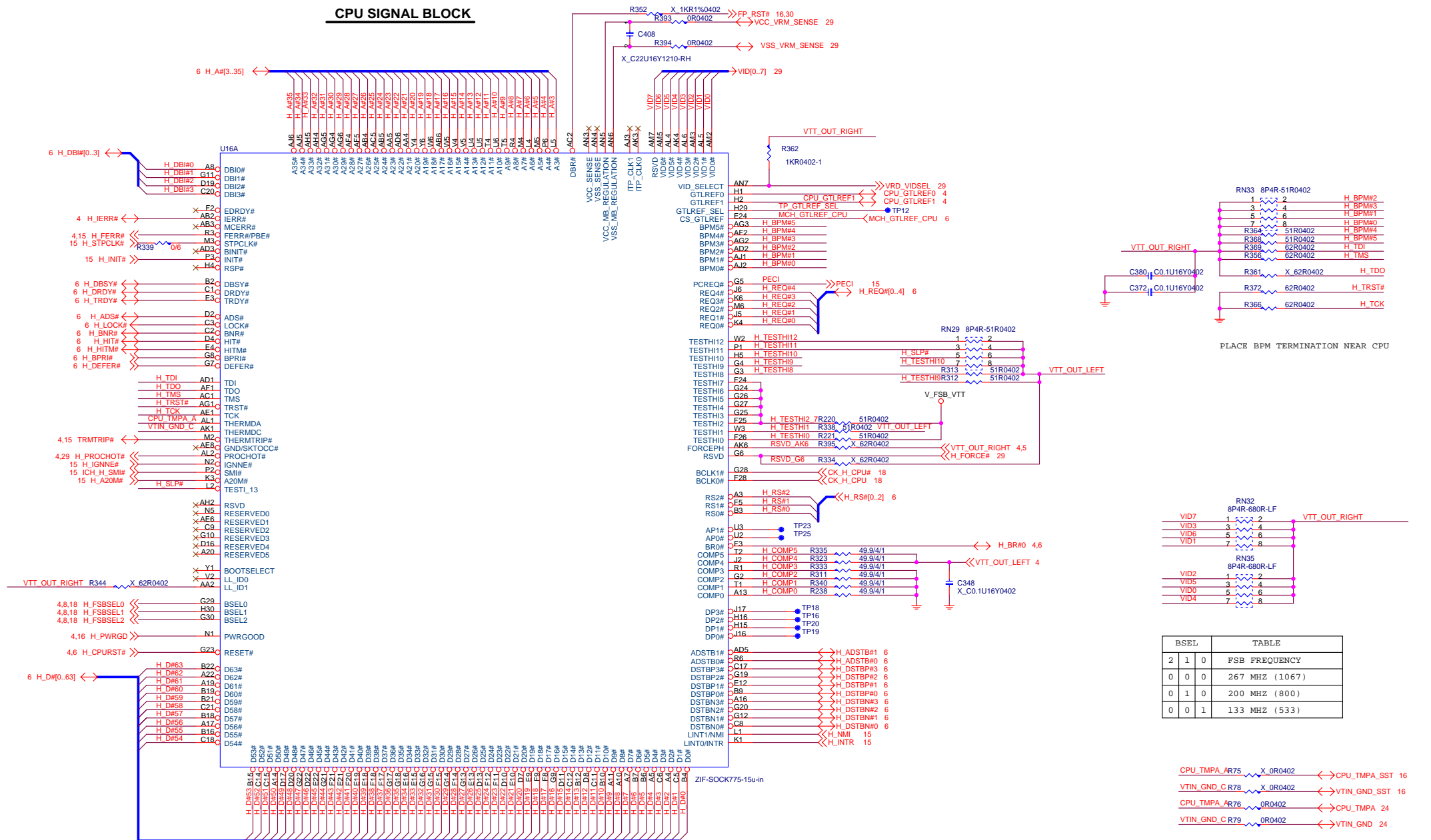
Controller: INTERSIL 6306 4 PHASES

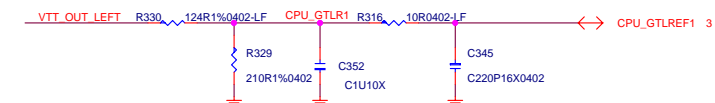
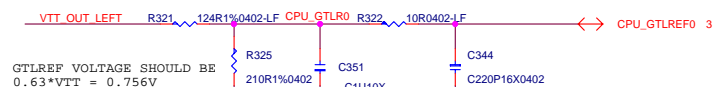
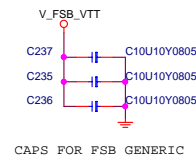
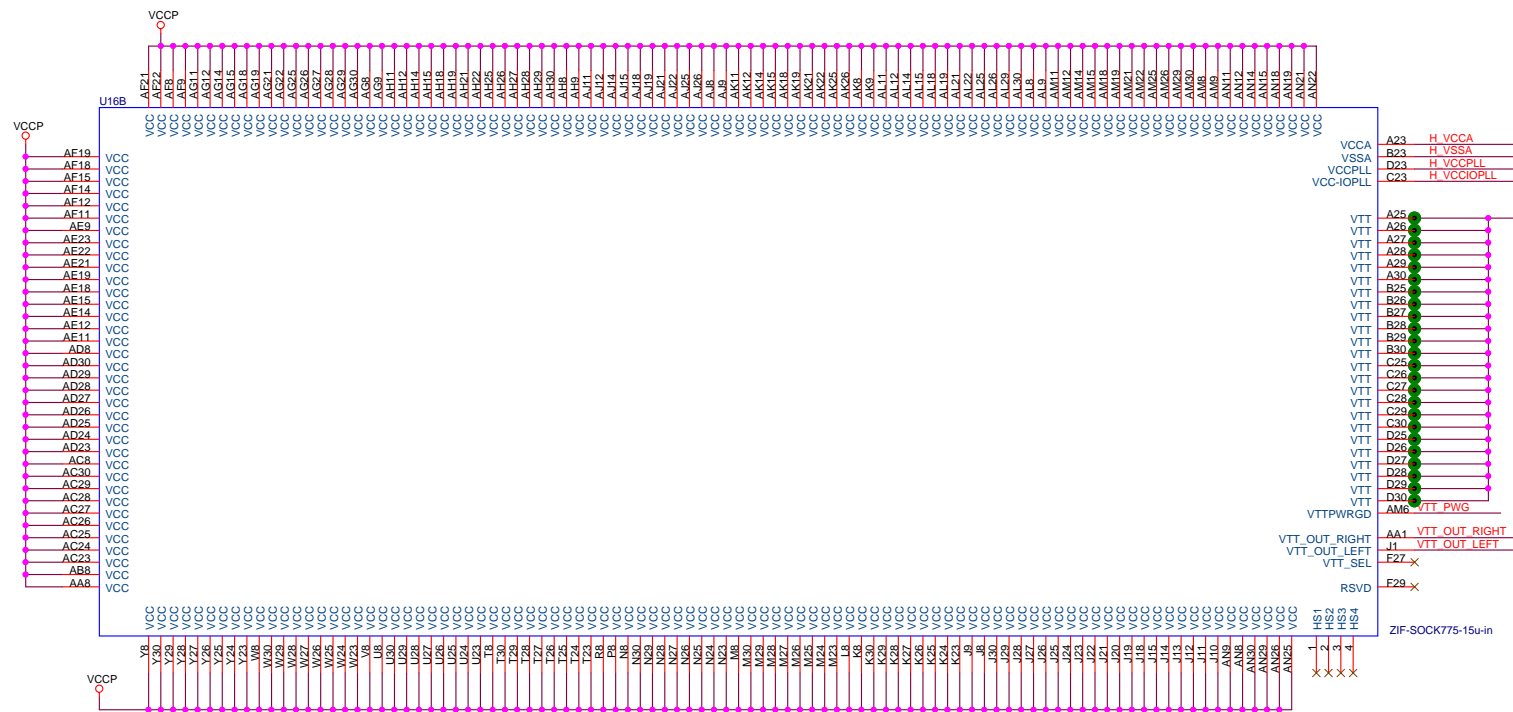
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Block Diagram



CPU SIGNAL BLOCK

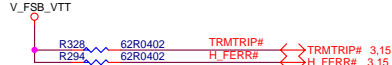




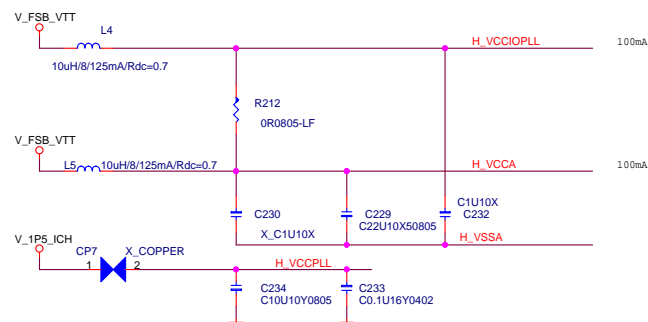
PLACE AT CPU END OF ROUTE



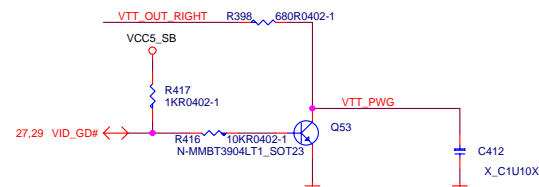
PLACE AT ICH END OF ROUTE



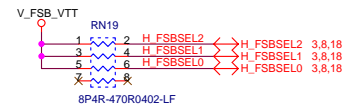
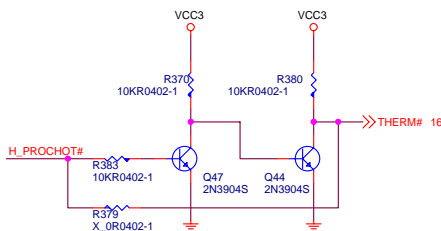
PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET
TRACE WIDTH TO CAPS MUST BE SMALLER THAN 12MILS



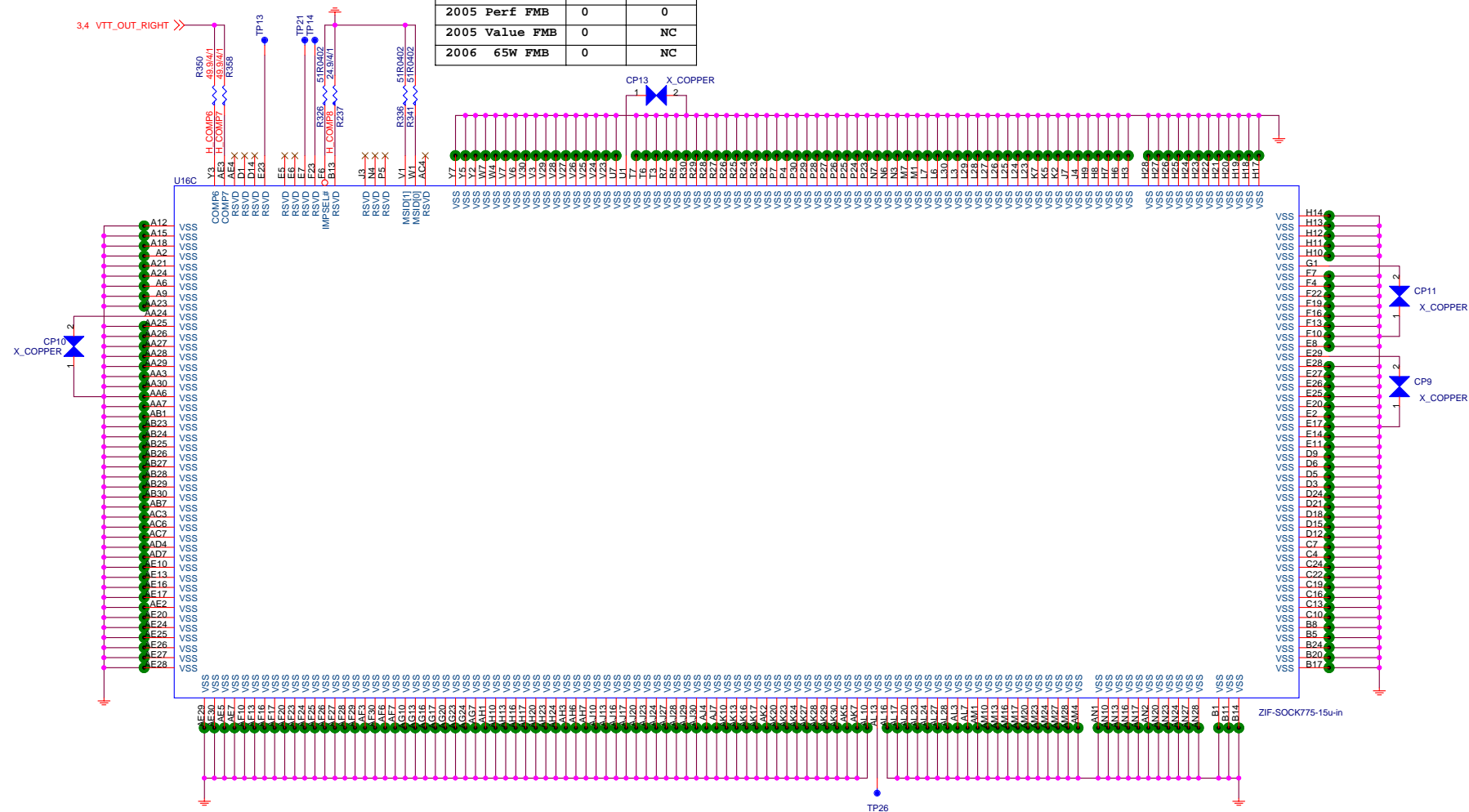
VTT_PWG SPEC :
High > 0.9V
Low < 0.3V
Trise < 150ns



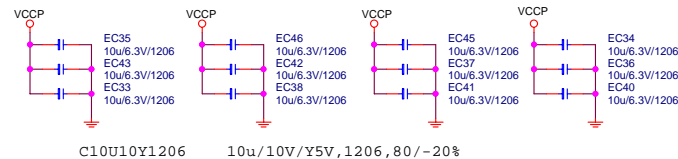
FSBSEL RESISTOR CAN BE REMOVED IF ONLY TEJAS AND CEDAR MILL ARE SUPPORTED



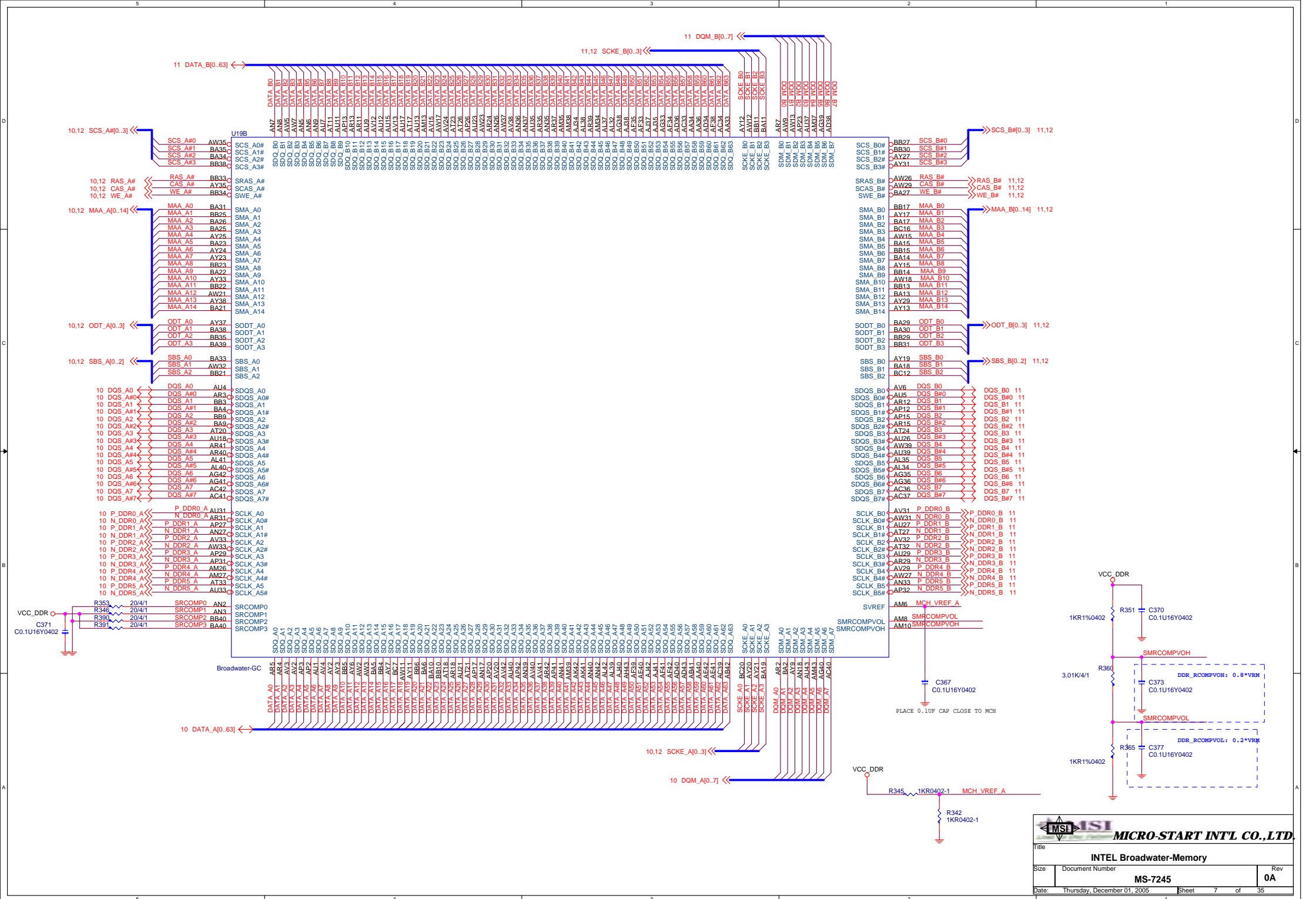
	MSID1	MSID0
2005 Perf FMB	0	0
2005 Value FMB	0	NC
2006 65W FMB	0	NC

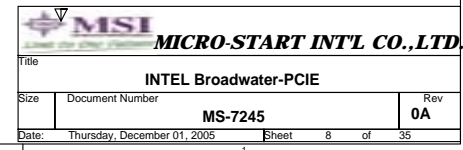


CPU DECOUPLING CAPACITORS



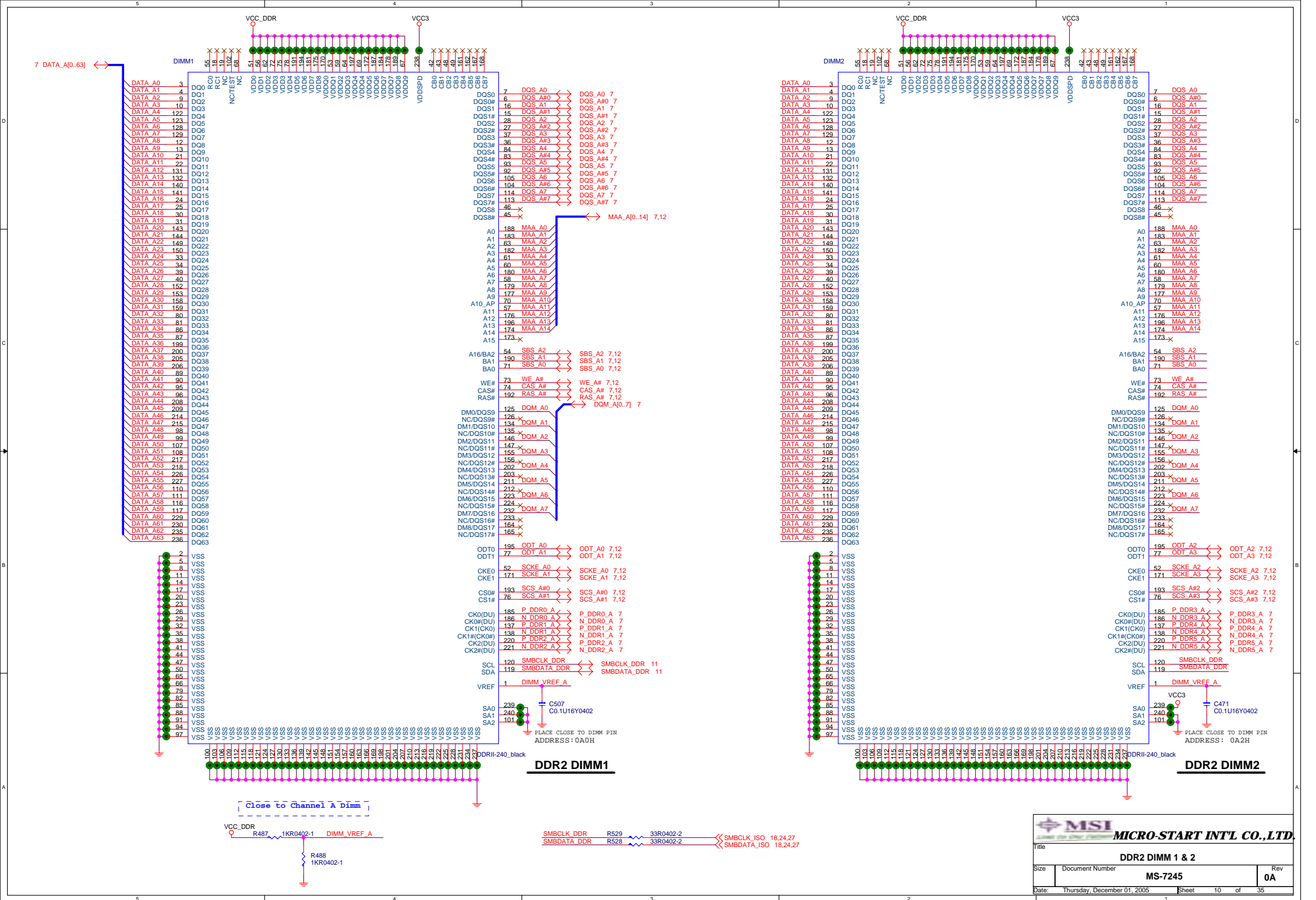
Place these caps within socket cavity

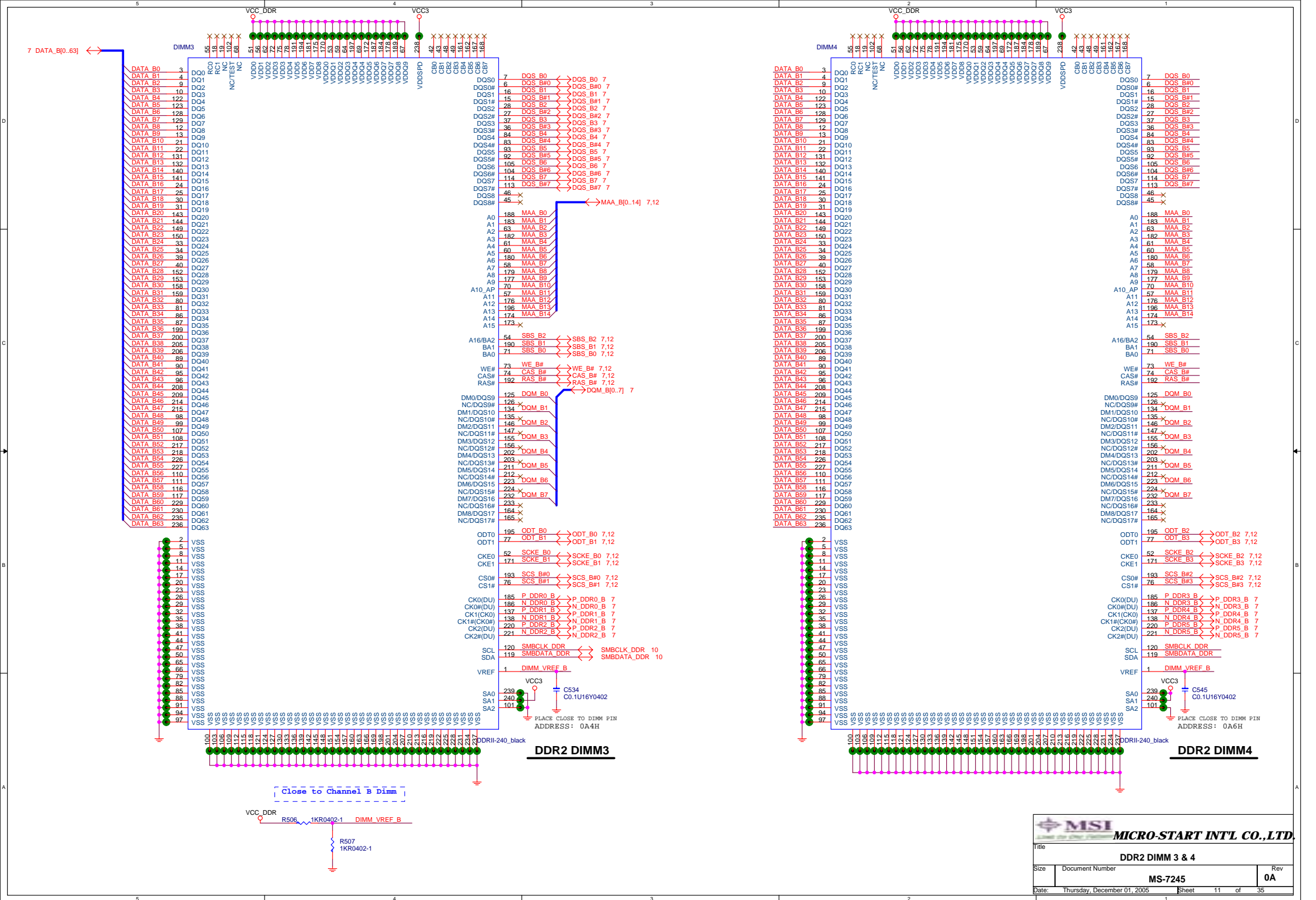




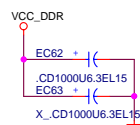
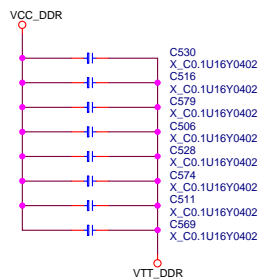
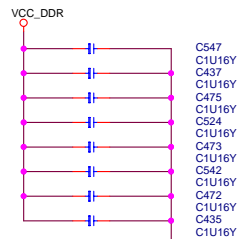
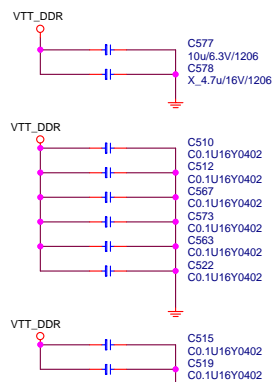
V_1P25_CORE



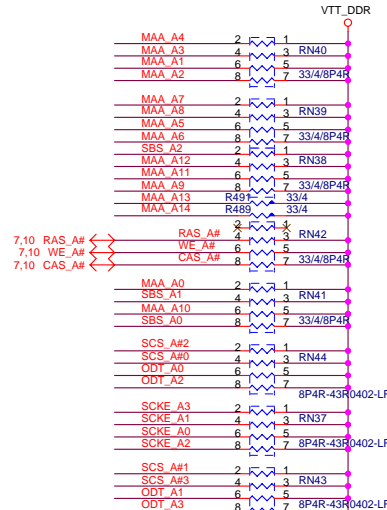
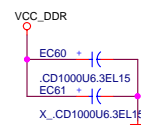
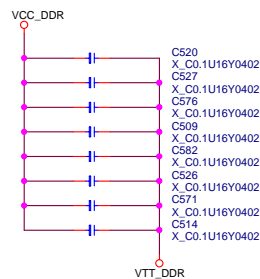
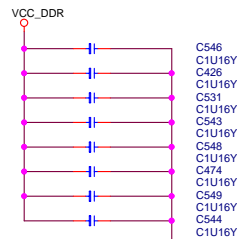
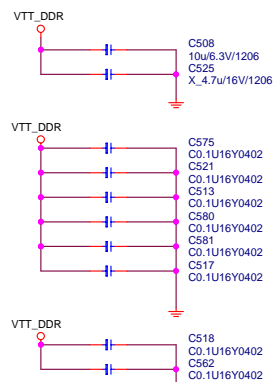




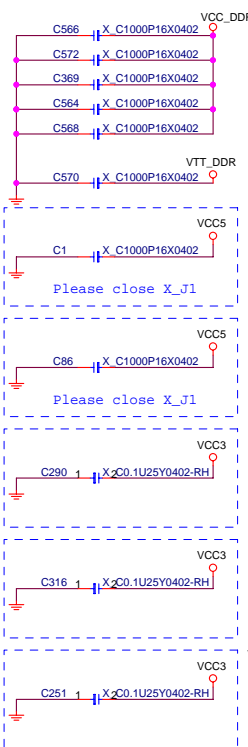
CHANNEL A V_SM_VTT DECOUPLING CAPS



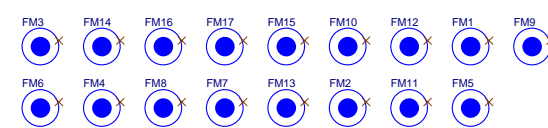
CHANNEL B V_SM_VTT DECOUPLING CAPS



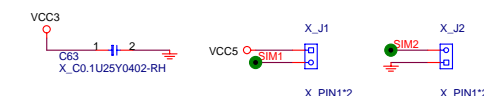
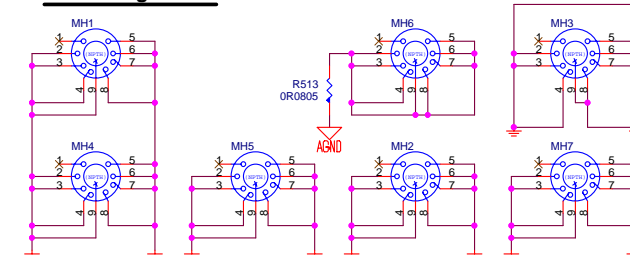
EMI Caps reserve



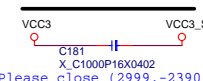
Optical Fiducial Marks



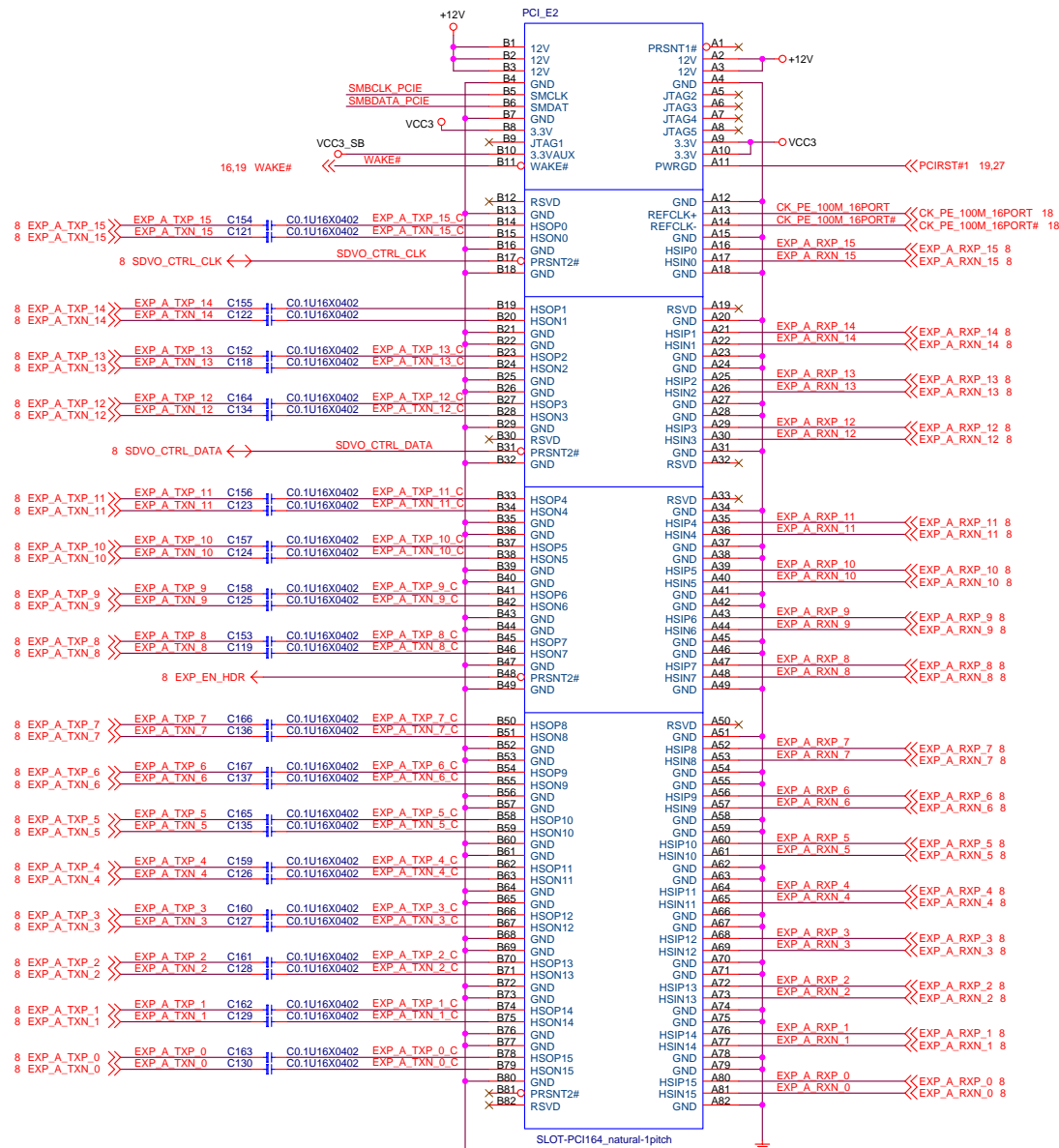
Mounting Holes



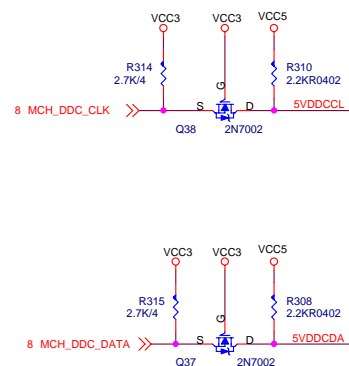
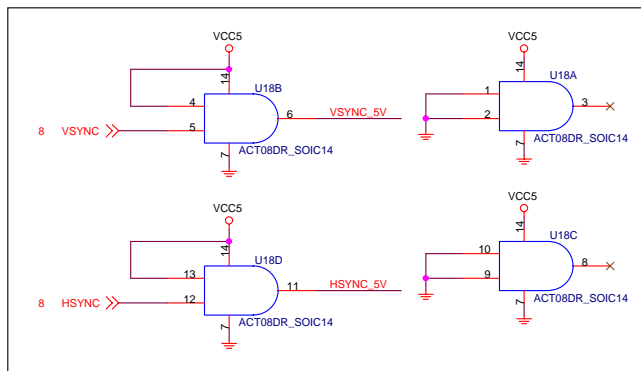
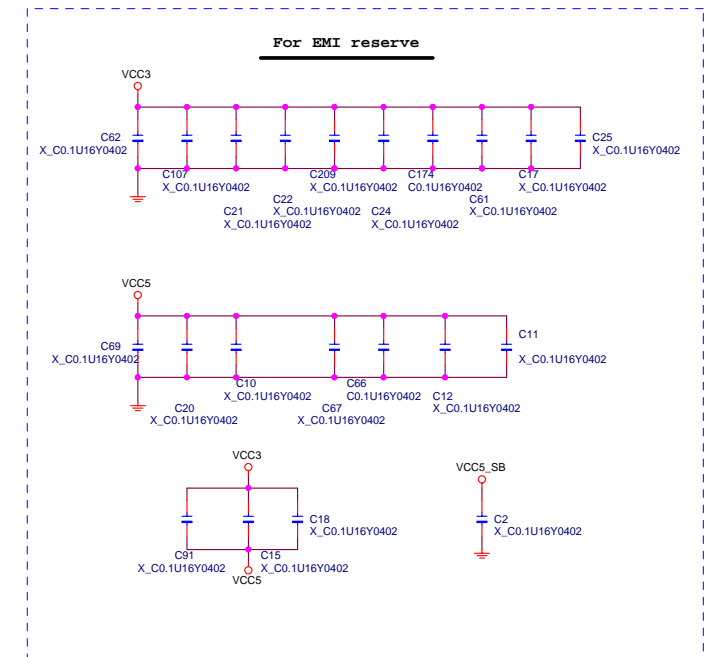
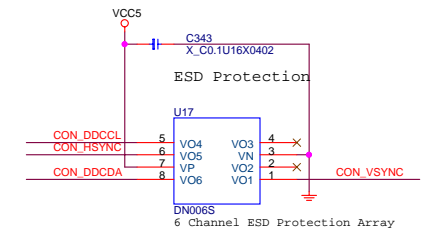
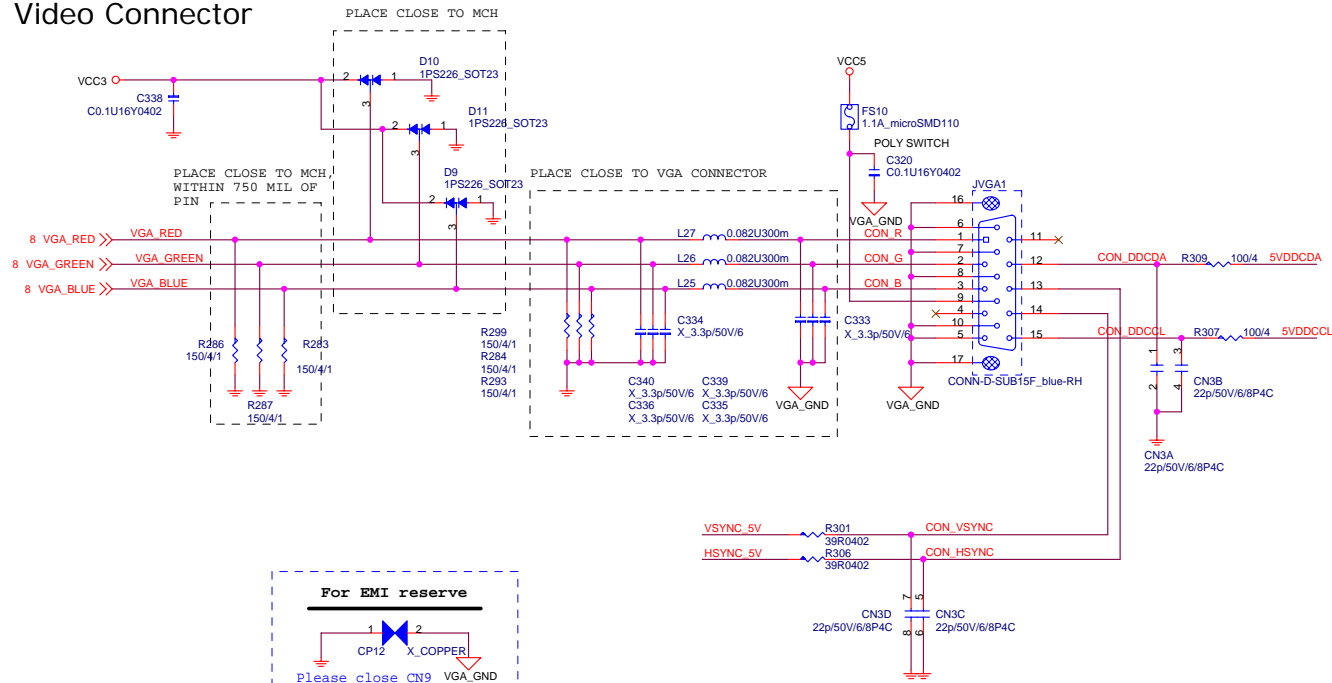
For EMI reserve

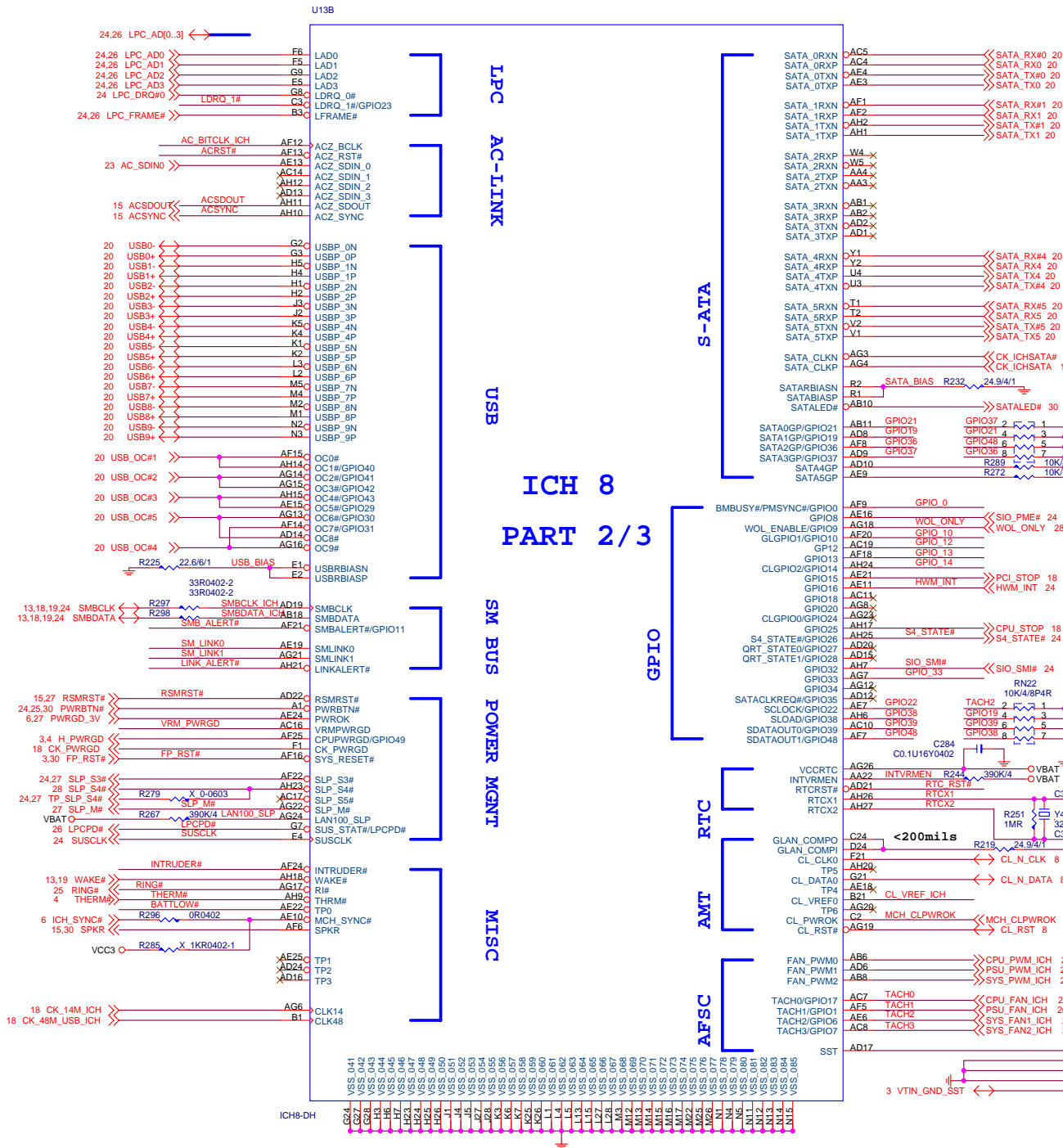


MSI MICRO-START INTL CO.,LTD.		
Title		
DDR TERMINATION		
Size	Document Number	Rev
	MS-7245	0A
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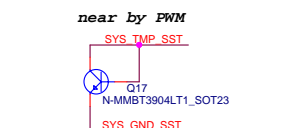
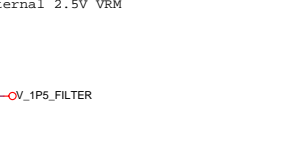
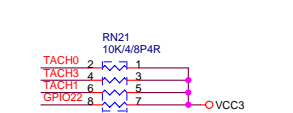
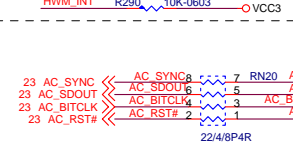
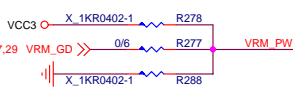
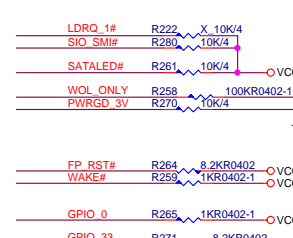
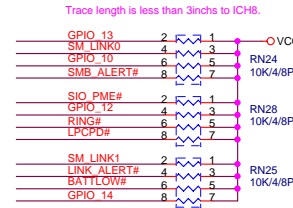
Video Connector



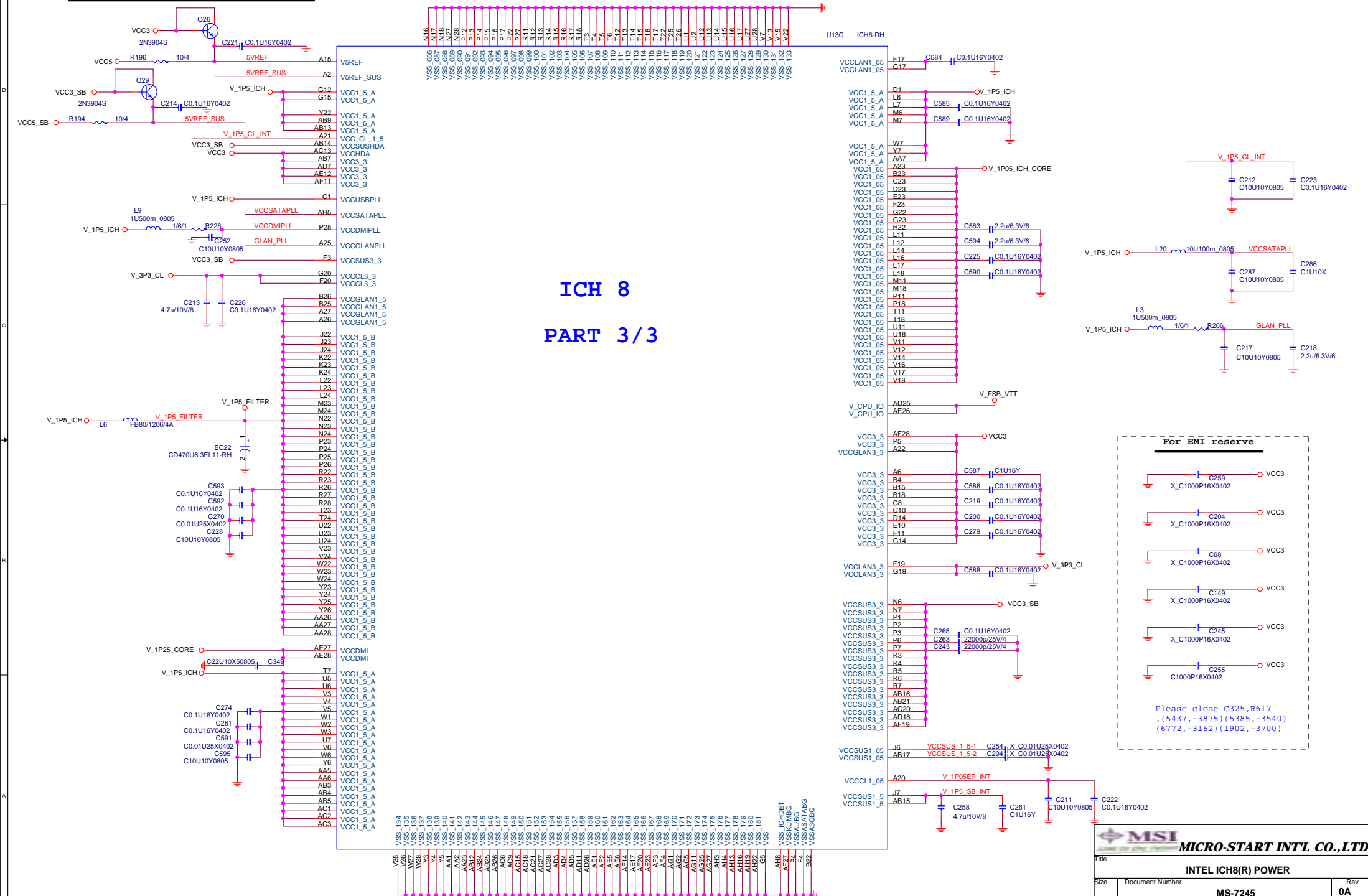


ICH8 PULL-UP RESISTORS

ALL COMPONENTS CLOSE TO ICH8
Trace length is less than 3inches to ICH8.



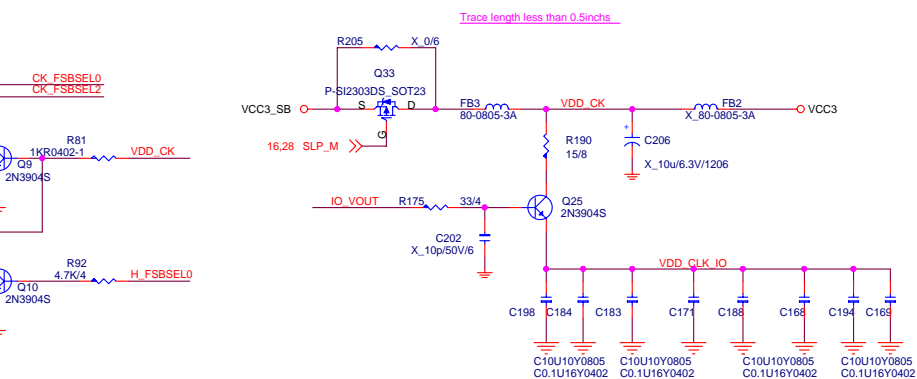
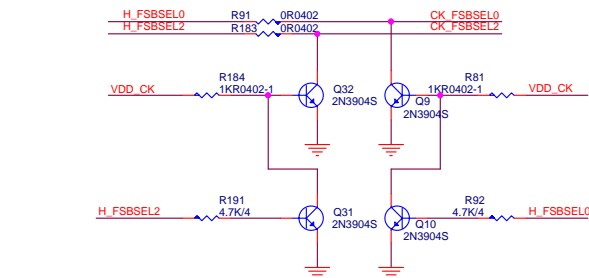
5VREF & 5VREF_SUS Sequencing Circuit



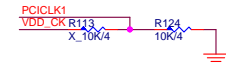
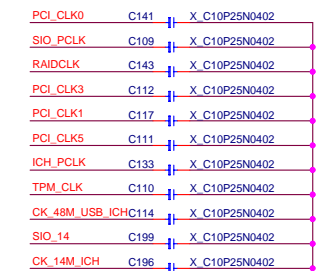
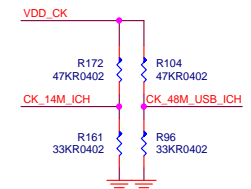
```

Please put all caps close CLK GEN.

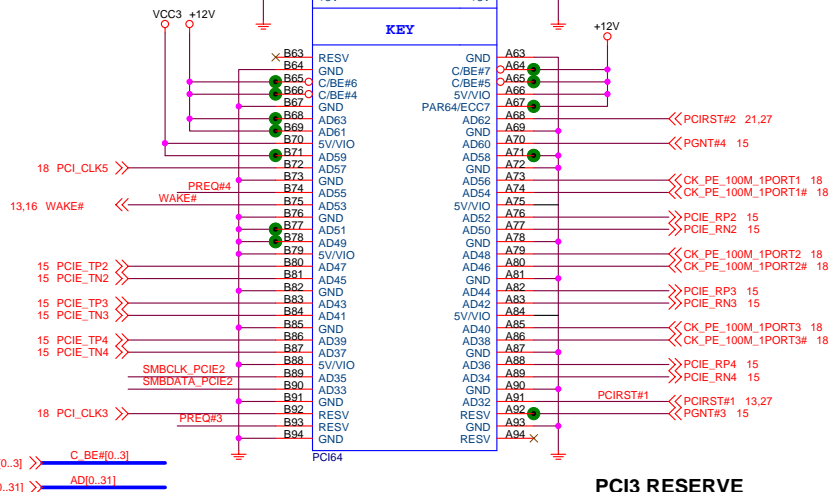
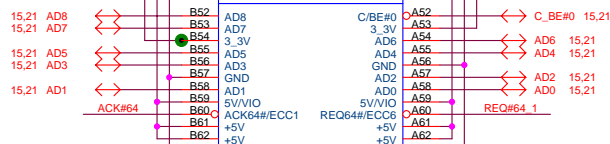
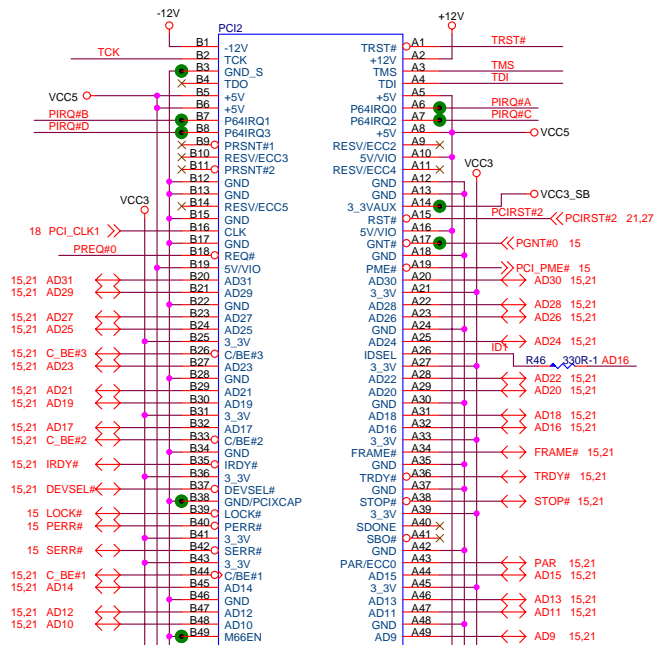
```



				PCI_STOP	R137	X	0R0402CK_PE_100M_ICH	
				CPU_STOP	R141	X	0R0402CK_PE_100M_ICH#	
3.4,8	H_FSBSEL1	H_FSBSEL1			R155	10K/4	FSB	
3.4,8	H_FSBSEL0	H_FSBSEL0			R95	10K/4	USB 48M	
		H_FSBSEL2			R181	10K/4	CLK 14M	



PCI1/PCIEXTENT

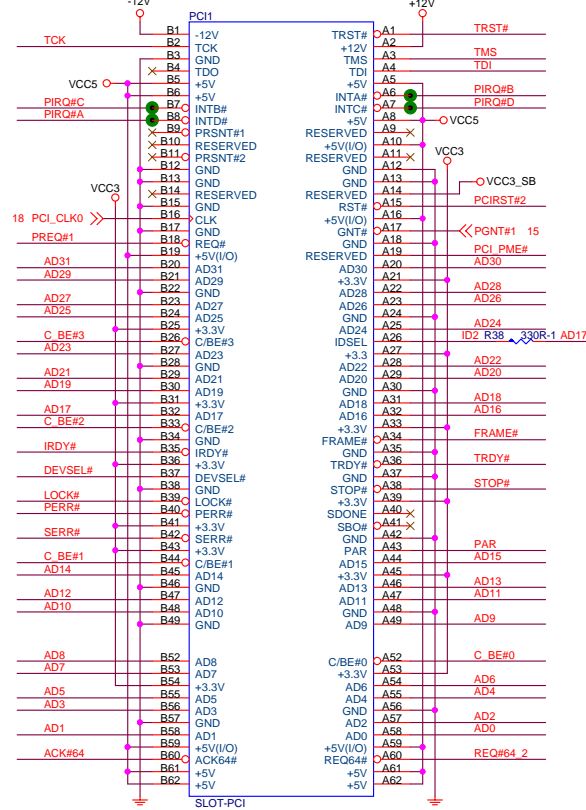


```

IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

```

```
PCI3 RESERVE
IDSEL = AD18
MASTER = PREQ#3
PIRQ#C
```

PCI SLOT 2 (PCI VER: 2.3 COMPLY)

```

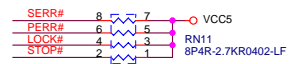
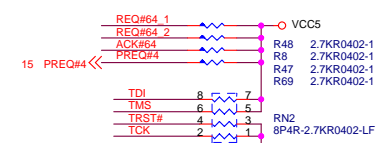
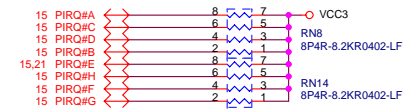
IDSEL = AD17
MASTER = PREQ#1
PIRQ#B

```

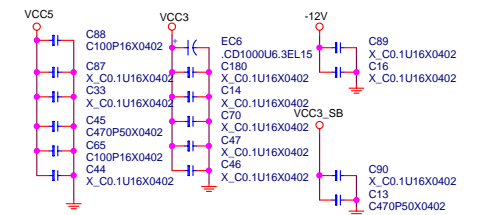
For EMI reserve

+12V
C84 X C0.01U25X040
Please close RN18

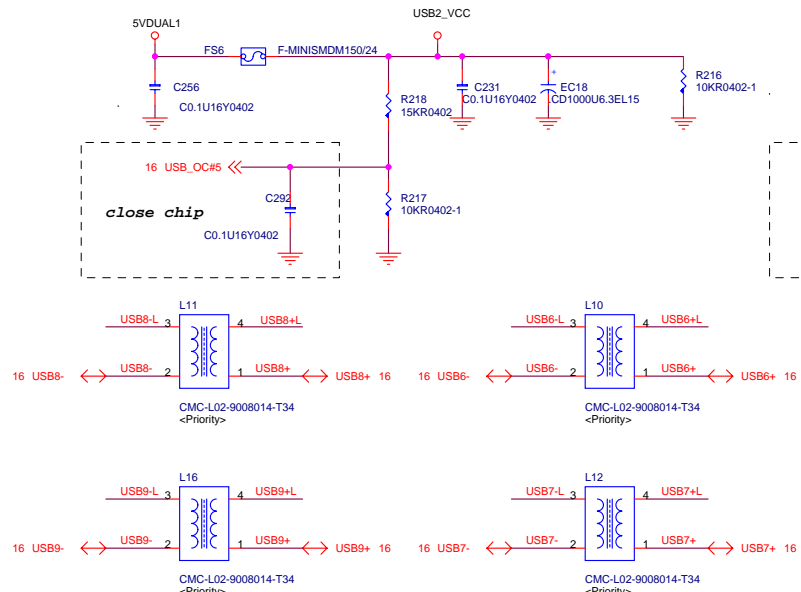
PCI PULL-UP / DOWN RESISTORS



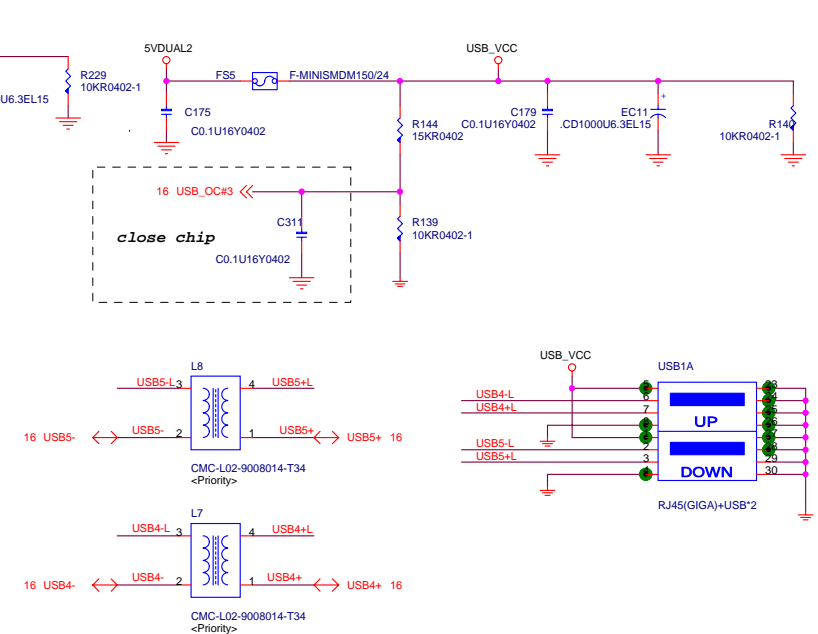
PCI SLOT DECOUPLING CAPACITORS



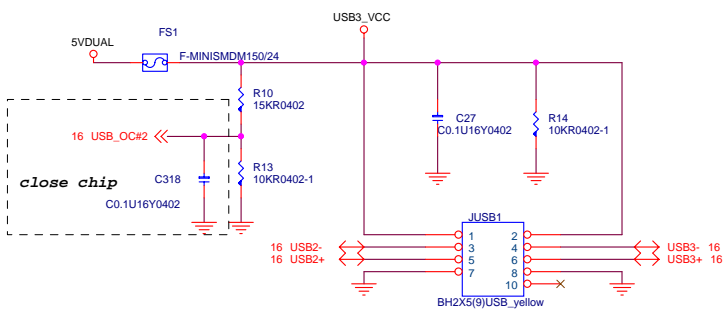
POWER CIRCUIT FOR USB PORT 6,7,8,9 (REAR)



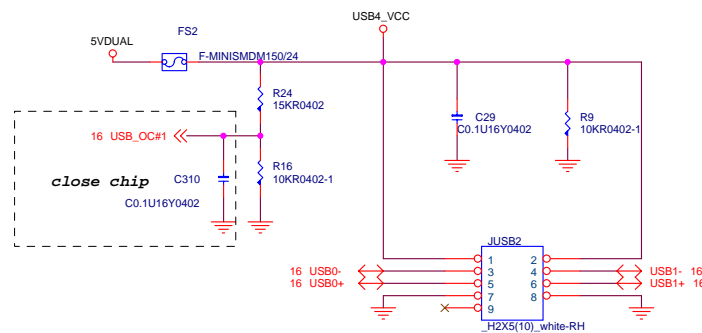
EXTERNAL USB PORT 4,5(REAR)



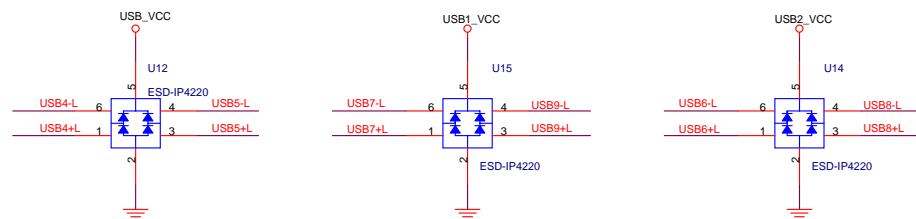
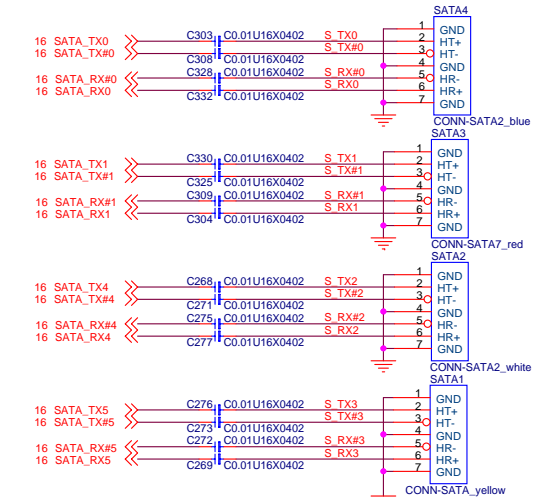
EXTERNAL USB PORT 2,3



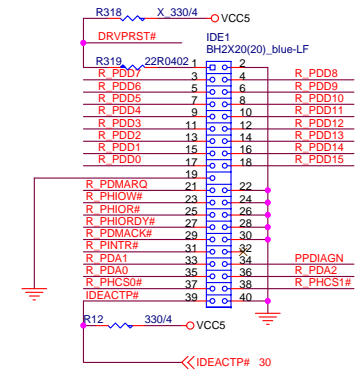
EXTERNAL USB PORT 0,1




SERIAL ATA CONNECTOR BLOCK

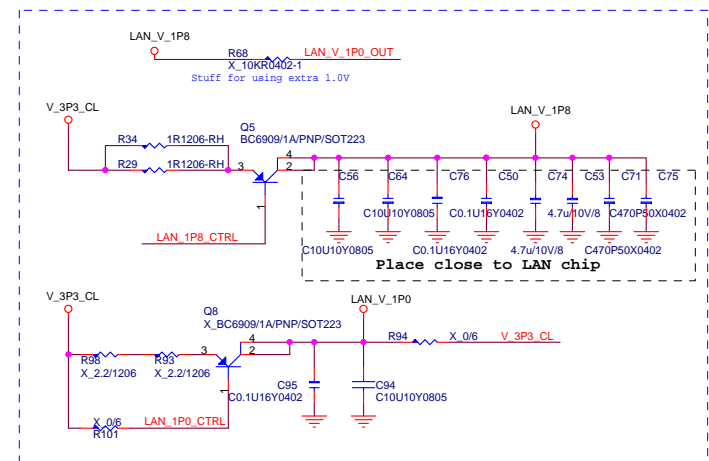
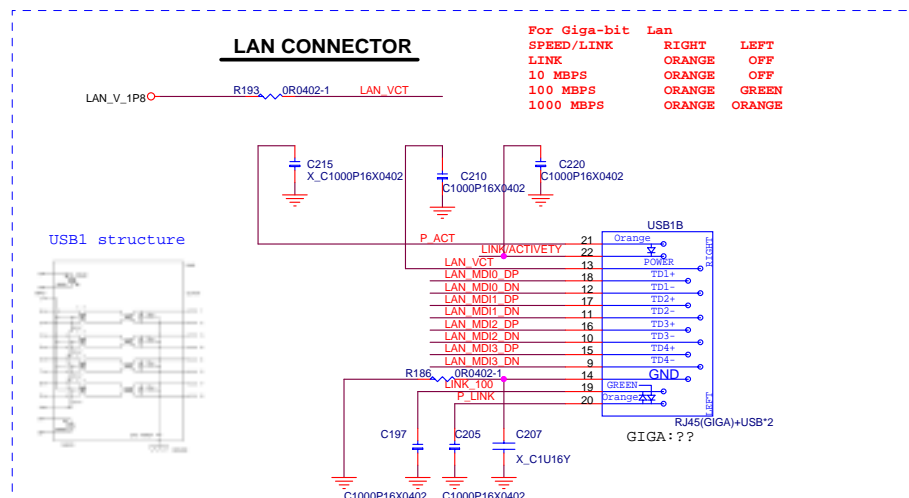
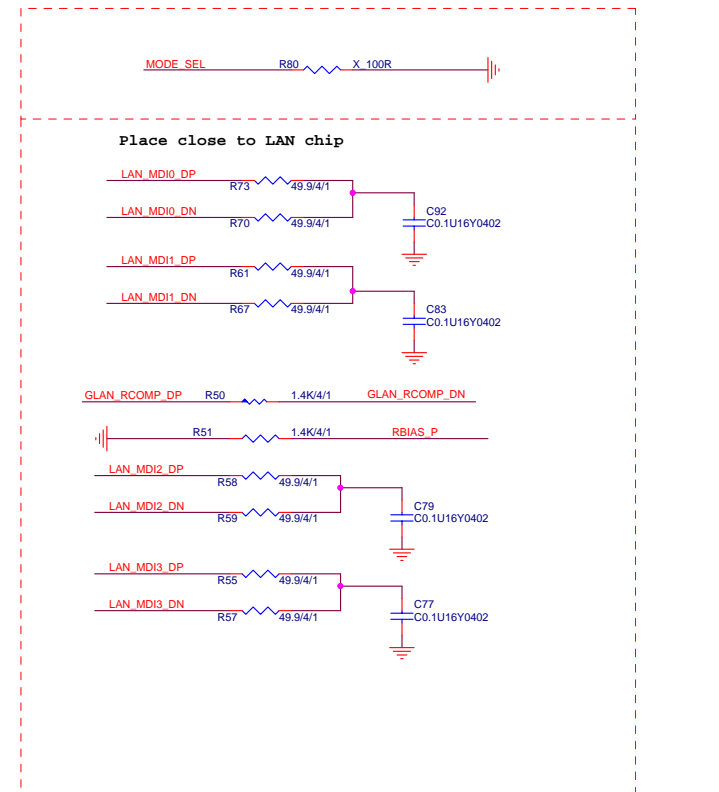
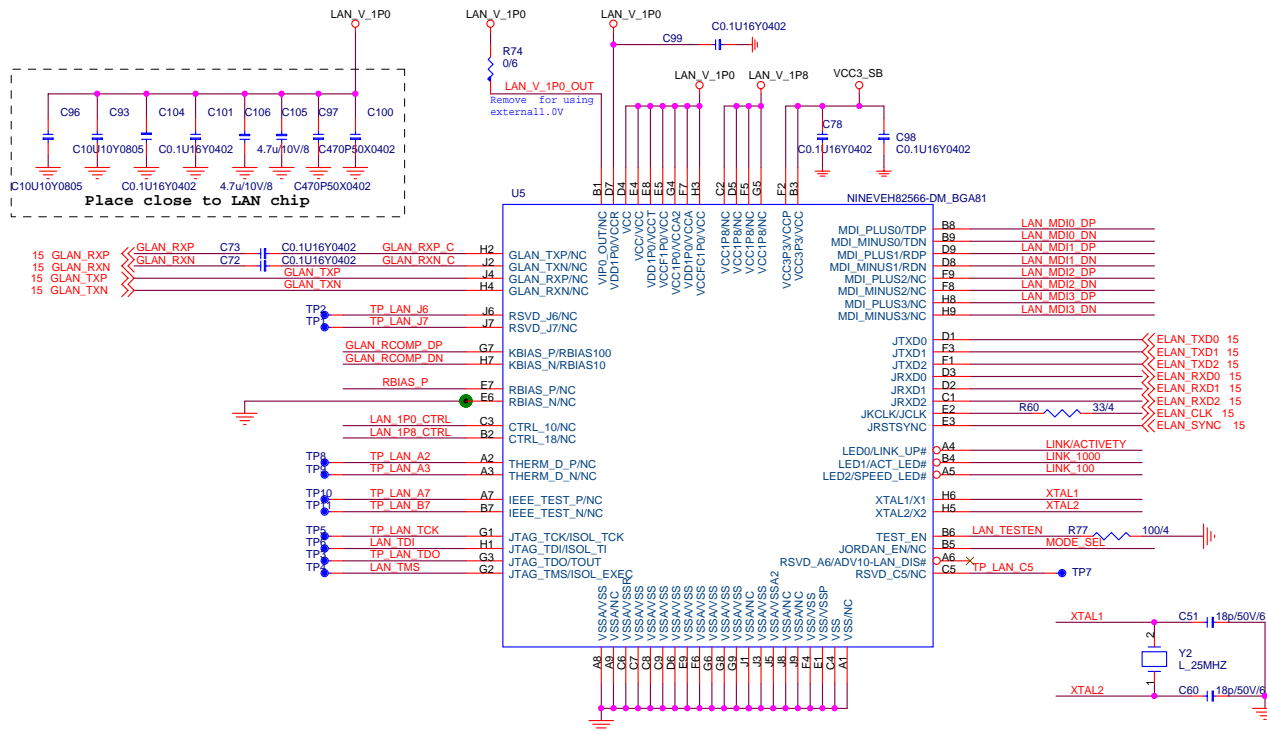


For EMI reserve
VCC5
C341 C1000P16X0402
please close SATA2 connector



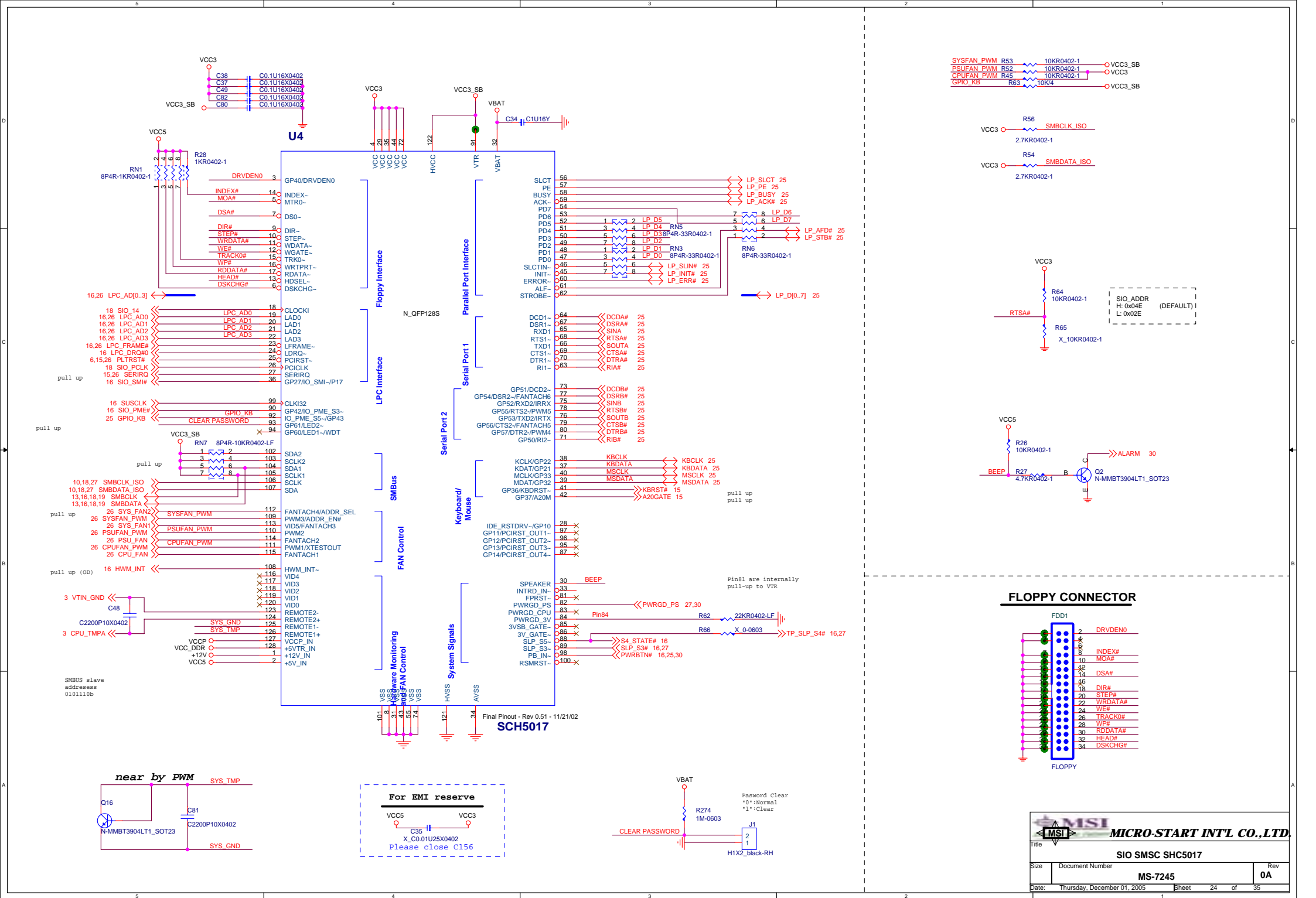
 MICRO-START INT'L CO.,LTD.				
Title				
VIA VT6410 RAID IDE				
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LAN - NINEVEH



ACT_LED	Link_LED
S0: LOW	S0: LOW
S1/S3/S4/S5: HIGH	S5: HIGH
	S1/S3/S4: WOL EN-->LOW WOL DIS-->HIGH

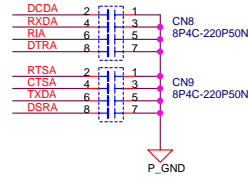
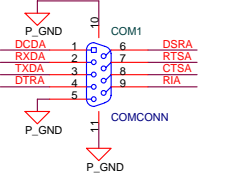




The schematic diagram shows the U24 component (GD75232_SSOP20) with the following connections:

- Pin 1:** Connected to +12V.
- Pin 2:** Connected to +12V.
- Pin 3:** Connected to DCD#.
- Pin 4:** Connected to SINA.
- Pin 5:** Connected to RTSA.
- Pin 6:** Connected to CTSA.
- Pin 7:** Connected to DSRA.
- Pin 8:** Connected to DTRA.
- Pin 9:** Connected to RTSA.
- Pin 10:** Connected to CTSA.
- Pin 11:** Connected to DSRA.
- Pin 12:** Connected to DIN1.
- Pin 13:** Connected to DIN2.
- Pin 14:** Connected to DIN3.
- Pin 15:** Connected to DOUT1.
- Pin 16:** Connected to DOUT2.
- Pin 17:** Connected to DOUT3.
- Pin 18:** Connected to DTRA.
- Pin 19:** Connected to +12V.
- Pin 20:** Connected to +12V.

The signals DCD#, SINA, RTSA, CTSA, DSRA, DTRA, RTSA, CTSA, DSRA, DIN1, DIN2, DIN3, DOUT1, DOUT2, DOUT3, and DTRA are also connected to the D14 (LS4148-GS08_LL34) and D13 (LS4148-GS08_LL34) components.

[illegible]

PH2*5(-10)

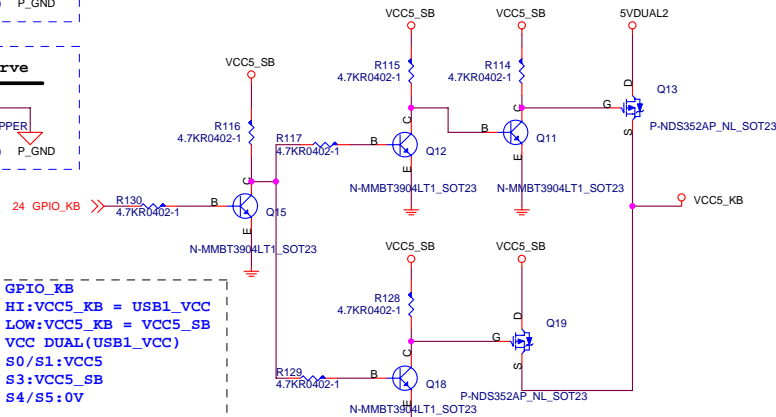
[illegible]

For EMI reserve

1 2
CP5 X_COPPER
Please close C139 P_GND

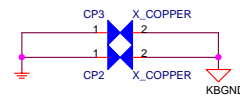
For EMI reserve

1 2
CP4 X_COPPER
Please close C139 P_GND

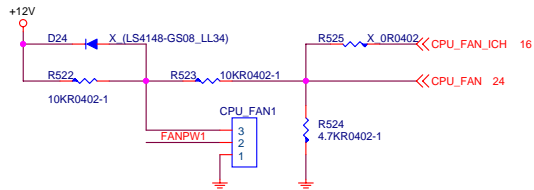
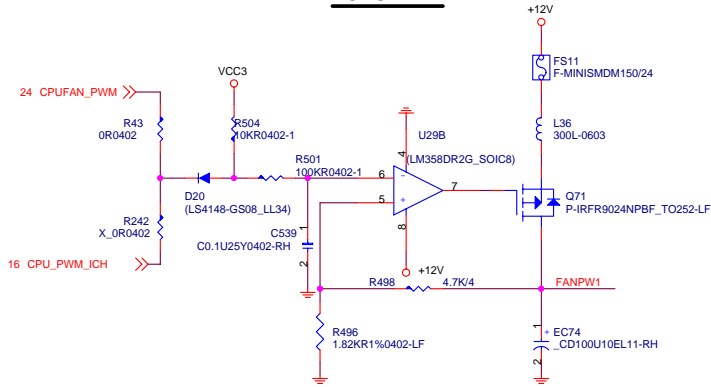


The schematic diagram illustrates the USB interface circuit for the C270P16X0402 module. It shows the connection between the module's pins and external components:

- Power Supply:** VCC5_MS and VCC5KB are connected to the module's power pins. A 5V regulator (FS9) provides 5V from a 5VDUAL2 source.
- Data Lines:** MSDATA, MSLCK, KBDATA, and KBCLK are connected to the module's data pins. These lines pass through resistors (R239, R240) and capacitors (C305, C323).
- Grounding:** The module's ground pins are connected to a common ground plane (KBGND).
- Capacitors:** Various capacitors (C299, C307, C315, C324, C278) are used for decoupling and signal conditioning.
- Resistors:** Resistors (R239, R240, R266) are used for current limiting and signal termination.

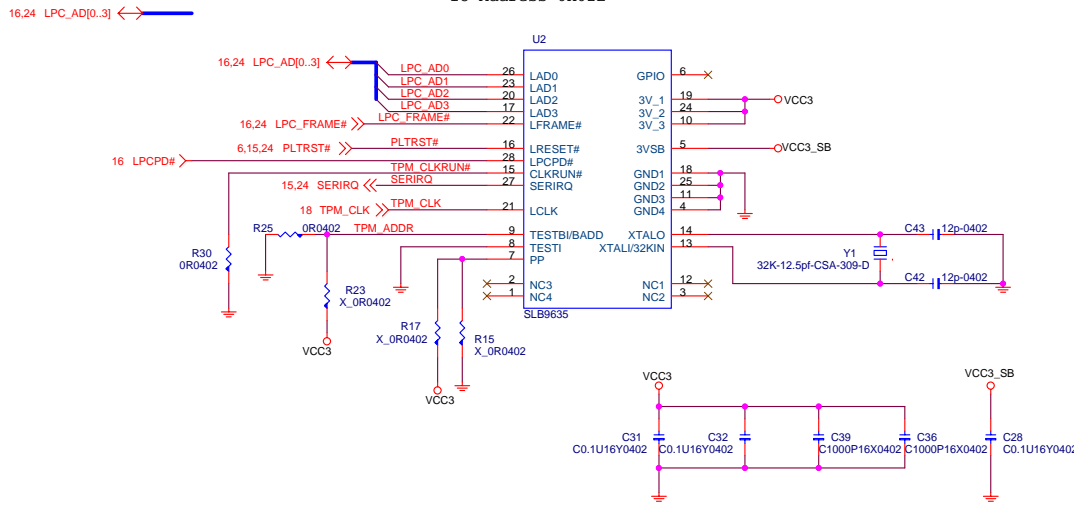


CPU FAN

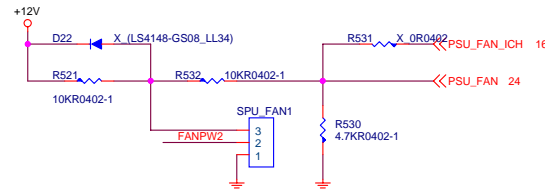
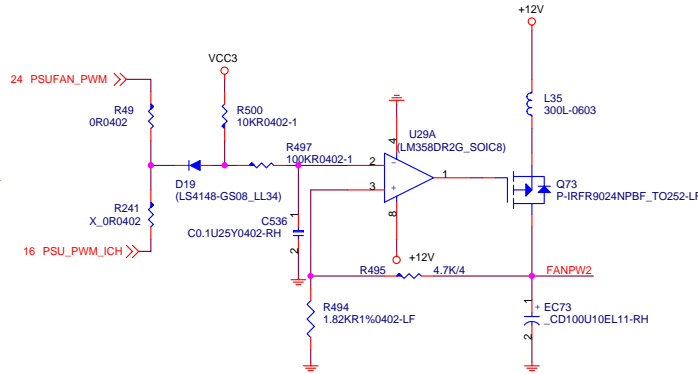


TPM 1.2

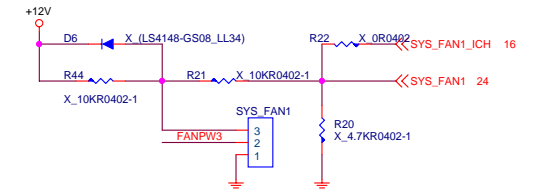
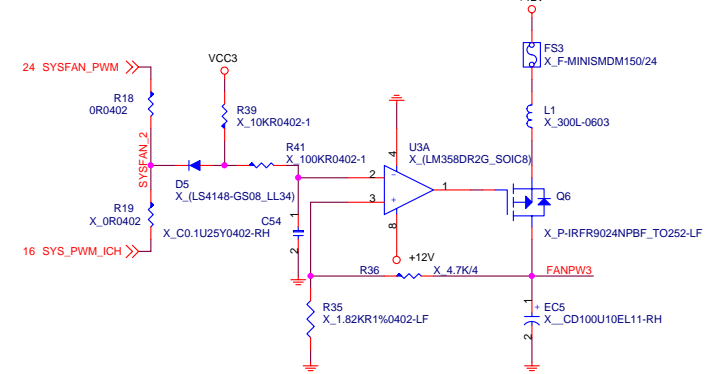
IO Address: 0x02E



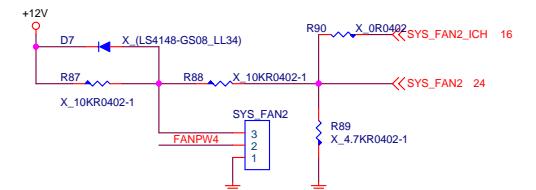
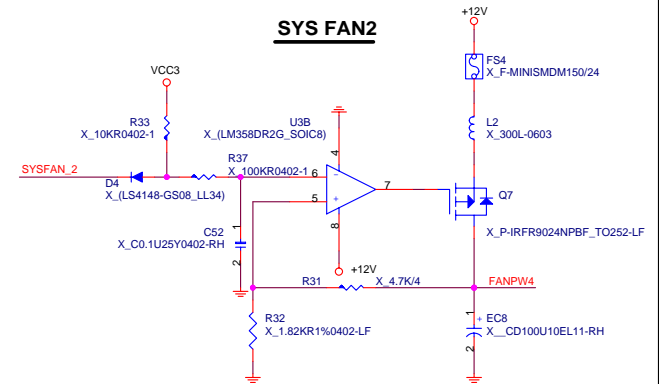
PSU FAN



SYS FAN1



SYS FAN2



For EMI reserve

VCC5
C346 C0.1U16Y0402

Please close (-1905 -1465)

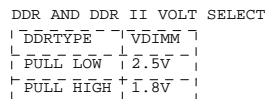
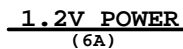
For EMI reserve

VCC5
C85 C0.1U16Y0402

Please close (-2450 5020)

3VSB MODE SELECT	
3VSB MODE	3VDLDEC#
SINGLE MOSFET	PULL HIGH
DUAL MOSFET	PULL LOW

VDIMM MODE	EXTRAM
LINEAR REGULATOR	PULL LOW
PWM REGULATOR	PULL HIGH

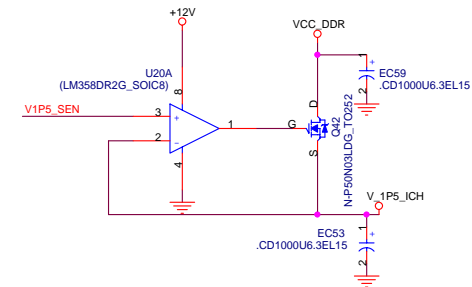
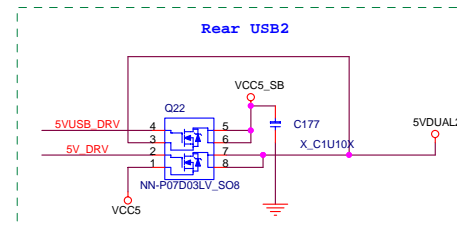
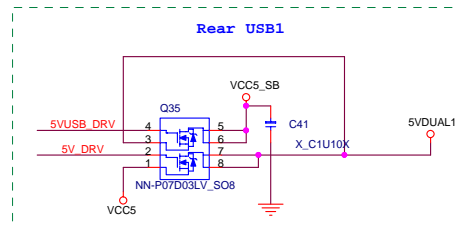


The schematic diagram for the 'FRONT USB' module shows the following connections:

- Pin 4:** Connected to **5VUSB_DRV** and **5V_DRV**.
- Pin 3:** Connected to **5VUSB_DRV** and **5V_DRV**.
- Pin 2:** Connected to **5VUSB_DRV** and **5V_DRV**.
- Pin 1:** Connected to **5VUSB_DRV** and **5V_DRV**.
- Pin 5:** Connected to **VCC5_SB**.
- Pin 6:** Connected to **VCC5_SB**.
- Pin 7:** Connected to **5VDUAL**.
- Pin 8:** Connected to **5VDUAL**.

Additional components and labels include:

- C59:** C2200P10X0402 (Capacitor)
- C57:** X_C2200P10X0402 (Capacitor)
- U3:** NN-P07D03LV_SO8 (USB module)

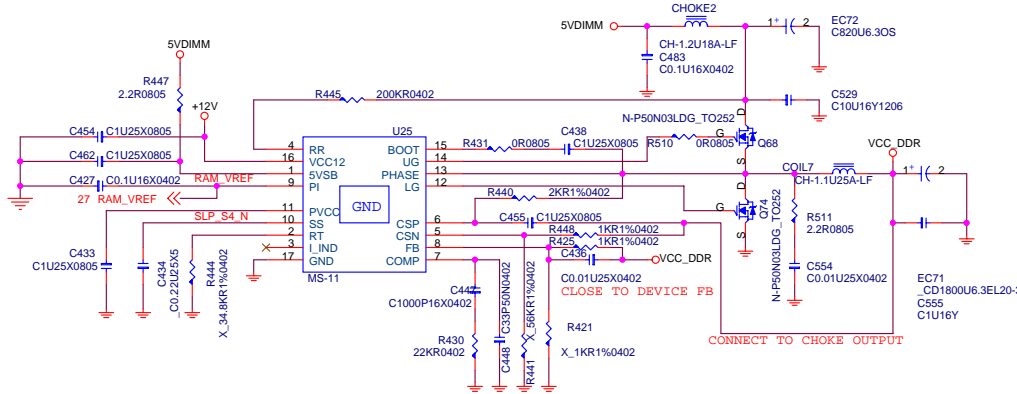
[illegible]

The schematic diagram illustrates the power supply section of the 6505A. It features a 5VDD supply connected to a network of capacitors (C452, C470, C466, C467) and transistors (Q61, Q63). The output is labeled RAM SBDV and RAM DRV. A ripple current of 2350mA is indicated. The circuit is powered by VCCS_SB and VCCS.

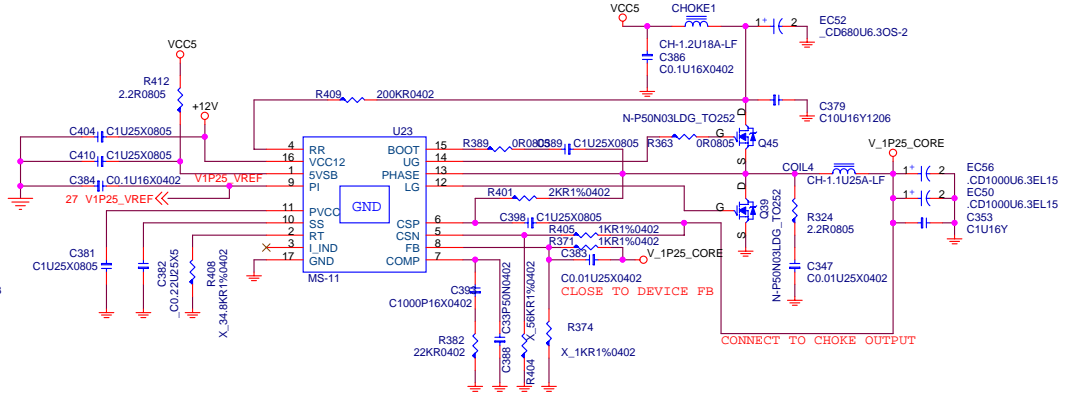


Title			
ACPI CONTROLLER MS7			
Size	Document Number	Rev	
	MS-7245	0A	
Date:	Thursday, December 01, 2005	Sheet	27 of 35

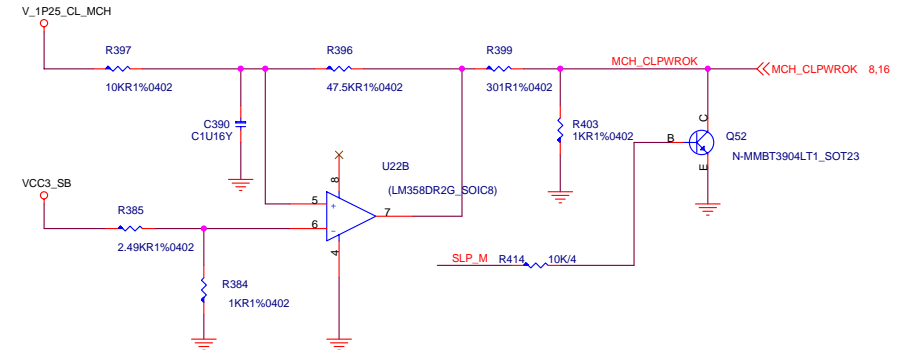
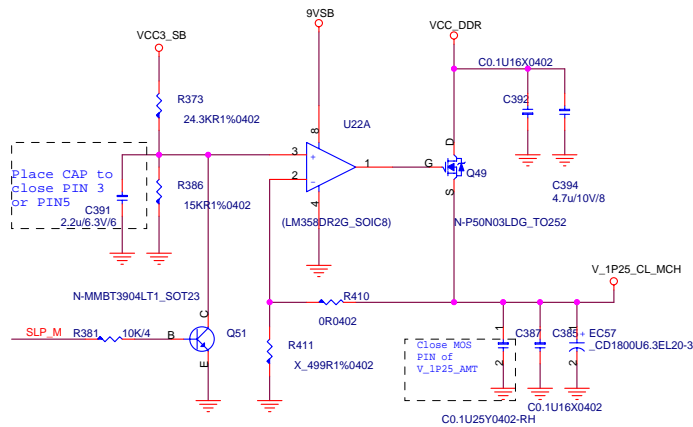
1.8V POWER (25A)



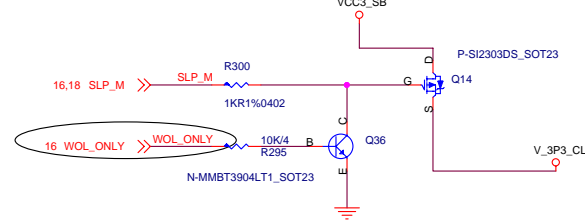
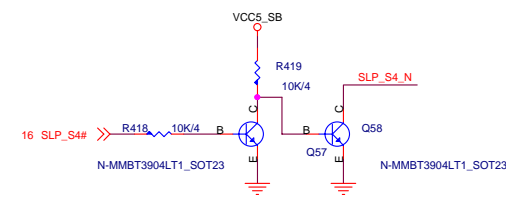
GMCH/ICH8 1.25V POWER (21.3A)



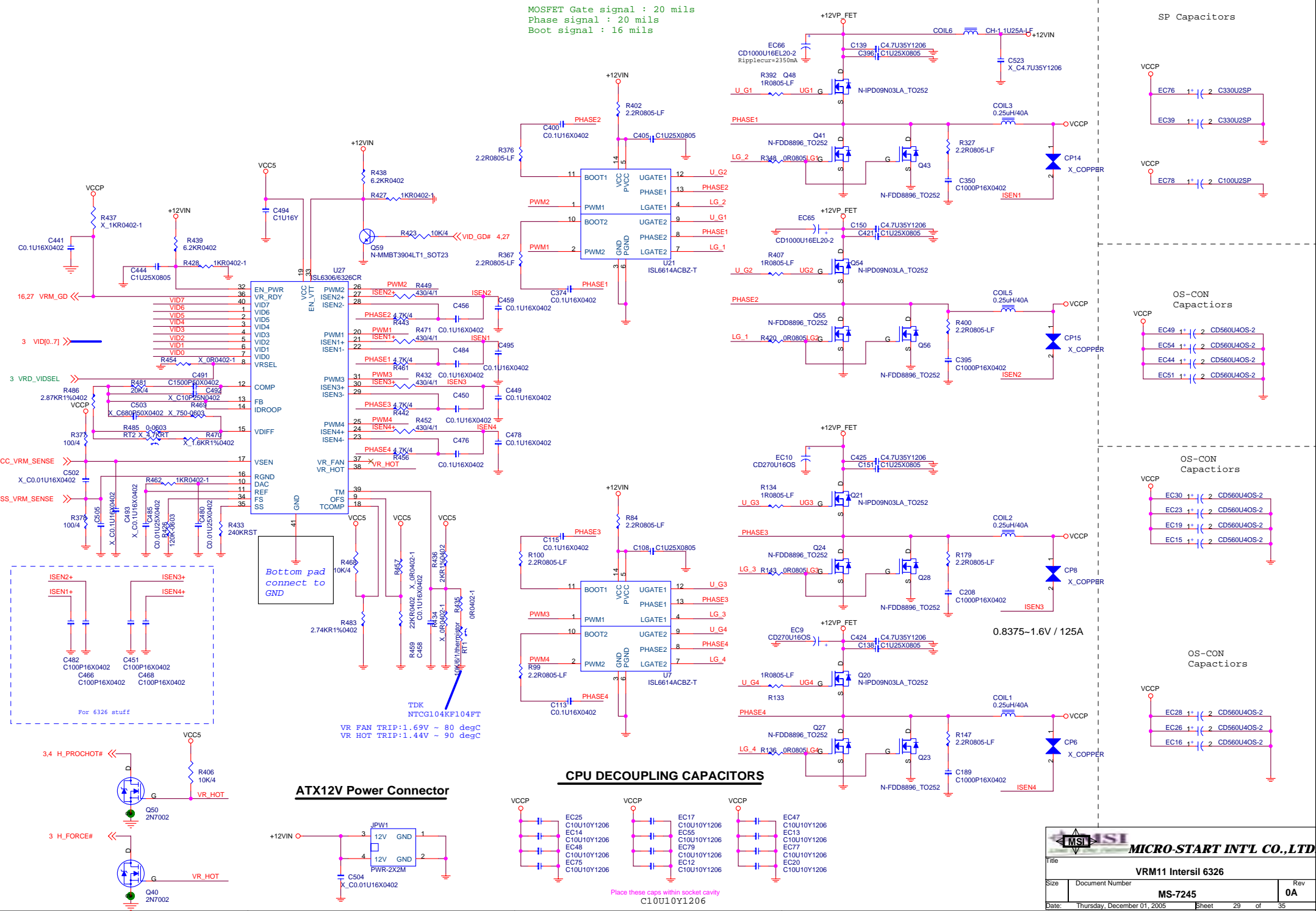
V_1P25_CL_MCH (3.8A)



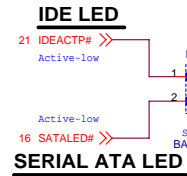
SLP_S4#
AMT Disable-->indicate ACPI S4 state,DRAM power off.
AMT Enable-->not be asserted ACPI S4 state,DRAM power ON
AMT Enable SLP_MH-->Control the overall power to Intel AMT during ACPI S3-S5.
S4_SATE#
AMT Enable-->indication of ACPI S4 state



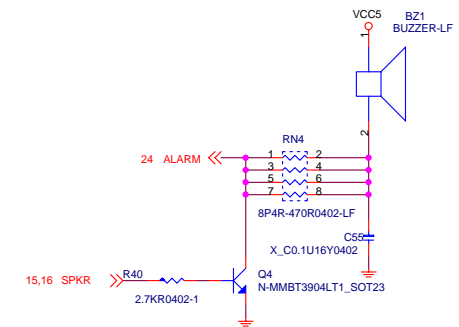
MOSFET Gate signal : 20 mils
Phase signal : 20 mils
Boot signal : 16 mils



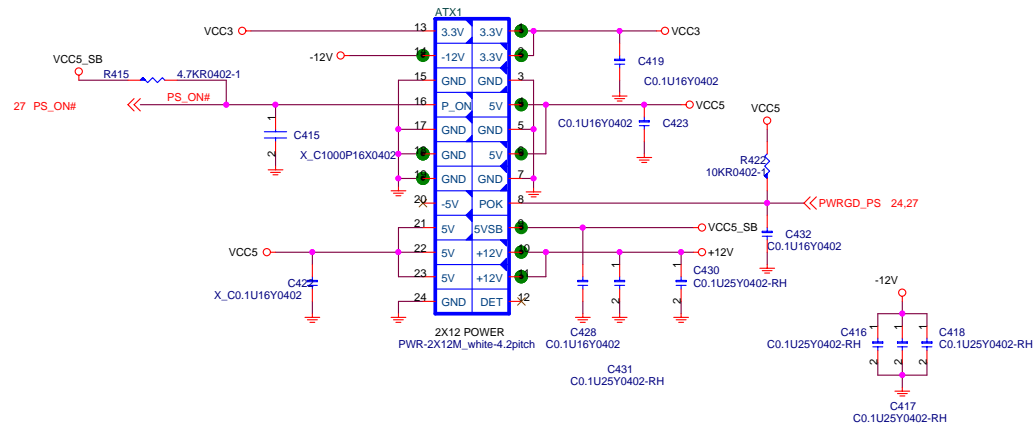
Front Panel



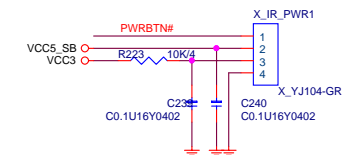
SPEAKER



ATX Connector



For NEC IR POWER



ICH8

GPIO Pin	Type	Default	Function	Power	MUXED/ UNMUXED	Pin-out
GPIO 0	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AF9
GPIO 1	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AF5
GPIO 2	I/O	GPI	PIRQ#E pull-up to VCC3 with 10K	VCC3		D5
GPIO 3	I/O	GPI	PIRQ#F pull-up to VCC3 with 10K	VCC3		F10
GPIO 4	I/O	GPI	PIRQ#G pull-up to VCC3 with 10K	VCC3		G11
GPIO 5	I/O	GPI	PIRQ#H pull-up to VCC3 with 10K	VCC3		F9
GPIO 6	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AE6
GPIO 7	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AC8
GPIO 8	I/O	GPI	SIO_PME# connect to SIO,pull_up VCC3_SB with 10k	VCC3_SB	UNMUXED	AE16
GPIO 9	I/O	MGPIO3	Pull-up to VCC3_SB with 10K directly	VCC3_SB	MUXED	AG18
GPIO 10	I/O	GPI	Pull-up to VCC3_SB with 10K directly	VCC3_SB	MUXED	AF20
GPIO 11	I/O	SMBALERT#	SMB_ALERT# pull-up to VCC3_SB with 10K	VCC3_SB		AF21
GPIO 12	I/O	GPI	Pull-up to VCC3_SB with 10K directly	VBT	UNMUXED	AC19
GPIO 13	I/O	GPI	Pull-up to VCC3_SB with 10K directly	VCC3_SB	UNMUXED	AF18
GPIO 14	I/O	GPI	Pull-up to VCC3_SB with 10K directly	VCC3_SB	MUXED	AH24
GPIO 15	I/O	GPO	PCI_STOP	VCC3_SB	UNMUXED	AE21
GPIO 16	I/O	GPO	SIO HWM_INT,pull_up VCC3 with 10K(change to GPI)		UNMUXED	AE11
GPIO 17	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AC7
GPIO 18	I/O	GPO	NC		UNMUXED	AC11
GPIO 19	I/O	GPI	Pull-up to VCC3 with 10K	VCC3		AD8
GPIO 20	I/O	GPO	NC		UNMUXED	AG8
GPIO 21	I/O	GPI	Pull-up to VCC3 with 10K	VCC3		AB11
GPIO 22	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AE7
GPIO 23	I/O	LDRQ1#	LDRQ_1# pull_up VCC3 with 10K	VCC3	MUXED	C3
GPIO 24	I/O	GPO	NC		MUXED	AG23
GPIO 25	I/O	GPO	CPU_STOP	3.3V_SB	UNMUXED	AH17
GPIO 26	I/O	GPO	S4 STATE			AH25
GPIO 27	I/O	GPO	NC	3.3V_SB		AD20
GPIO 28	I/O	GPO	NC			AD15
GPIO 29	I/O	OC5#	OC#3 connect to USB connector	3.3V_SB		AE15
GPIO 30	I/O	OC6#	OC#4 connect to USB connector	3.3V_SB		AG13
GPIO 31	I/O	OC7#	OC#4 connect to USB connector	3.3V_SB		AF14
GPIO 32	I/O	GPO	SIO_SMI# connect to SIO,pull up VCC3 with 10k	VCC3	UNMUXED	AH7
GPIO 33	I/O	GPO	Pull-up to VCC3 with 8.2K		UNMUXED	AG7
GPIO 34	I/O	GPO	NC		UNMUXED	AG12
GPIO 35	I/O	GPO	NC			AD12
GPIO 36	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AF8
GPIO 37	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AD9
GPIO 38	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AH6
GPIO 39	I/O	GPI	Pull-down to GND with 10K directly	VCC3		AC10
GPIO 40	I/O	OC1#	OC#1 connect to USB connector	VCC3		AH14
GPIO 41	I/O	OC2#	OC#2 connect to USB connector	VCC3		AG14
GPIO 42	I/O	OC3#	OC#2 connect to USB connector	VCC3		AG15
GPIO 43	I/O	OC4#	OC#3 connect to USB connector	VCC3		AH15
GPIO 48	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AF7
GPIO 49	I/O	CPU_PWRGD	H_PWRGD connect to CPU	VTT_OUT		AF25
GPIO 50	I/O	REQ1#	REQ1 pull-up to VCC5 with 10K	VCC5	MUXED	C16
GPIO 51	I/O	GNT1#	GNT1#		MUXED	A15
GPIO 52	I/O	REQ2#	REQ2 pull-up to VCC5 with 10K	VCC5	MUXED	B16
GPIO 53	I/O	GNT2#	GNT2#		MUXED	D17
GPIO 54	I/O	REQ3#	REQ3 pull-up to VCC5 with 10K	VCC5	MUXED	A9
GPIO 55	I/O	GNT3#	GNT3#		MUXED	B9

PCI Configuration

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI1 EXTENT	PIRQ#A PIRQ#B PIRQ#C PIRQ#D	PREQ#0 PGNT#0	AD16	PCI_CLK1
PCI2	PIRQ#B PIRQ#C PIRQ#D PIRQ#A	PREQ#1 PGNT#1	AD17	PCI_CLK0
VT6410	PIRQ#E	PREQ#2 PGNT#2	AD20	RAIDCLK
PCI3	RESERVED	PREQ#3 PGNT#3	AD18	PCI_CLK3

DDRII DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	0A0H	SCLK_A0/SCLK_A0# SCLK_A1/SCLK_A1# SCLK_A2/SCLK_A2#
DIMM 2	0A2H	SCLK_A3/SCLK_A3# SCLK_A4/SCLK_A4# SCLK_A5/SCLK_A5#
DIMM 3	0A4H	SCLK_B0/SCLK_B0# SCLK_B1/SCLK_B1# SCLK_B2/SCLK_B2#
DIMM 4	0A6H	SCLK_B3/SCLK_B3# SCLK_B4/SCLK_B4# SCLK_B5/SCLK_B5#

SIO SCH5017


PIN NAME	PIN#	USAGE	Input/Output
GP42	92	GPIO_KB	OUTPUT
GP27	36	SIO_SMI#	OUTPUT
GP43	90	SIO_PME#	OUTPUT
GP61	93	CLEAR_PASSWORD	INPUT

SMBus DISTRIBUTION

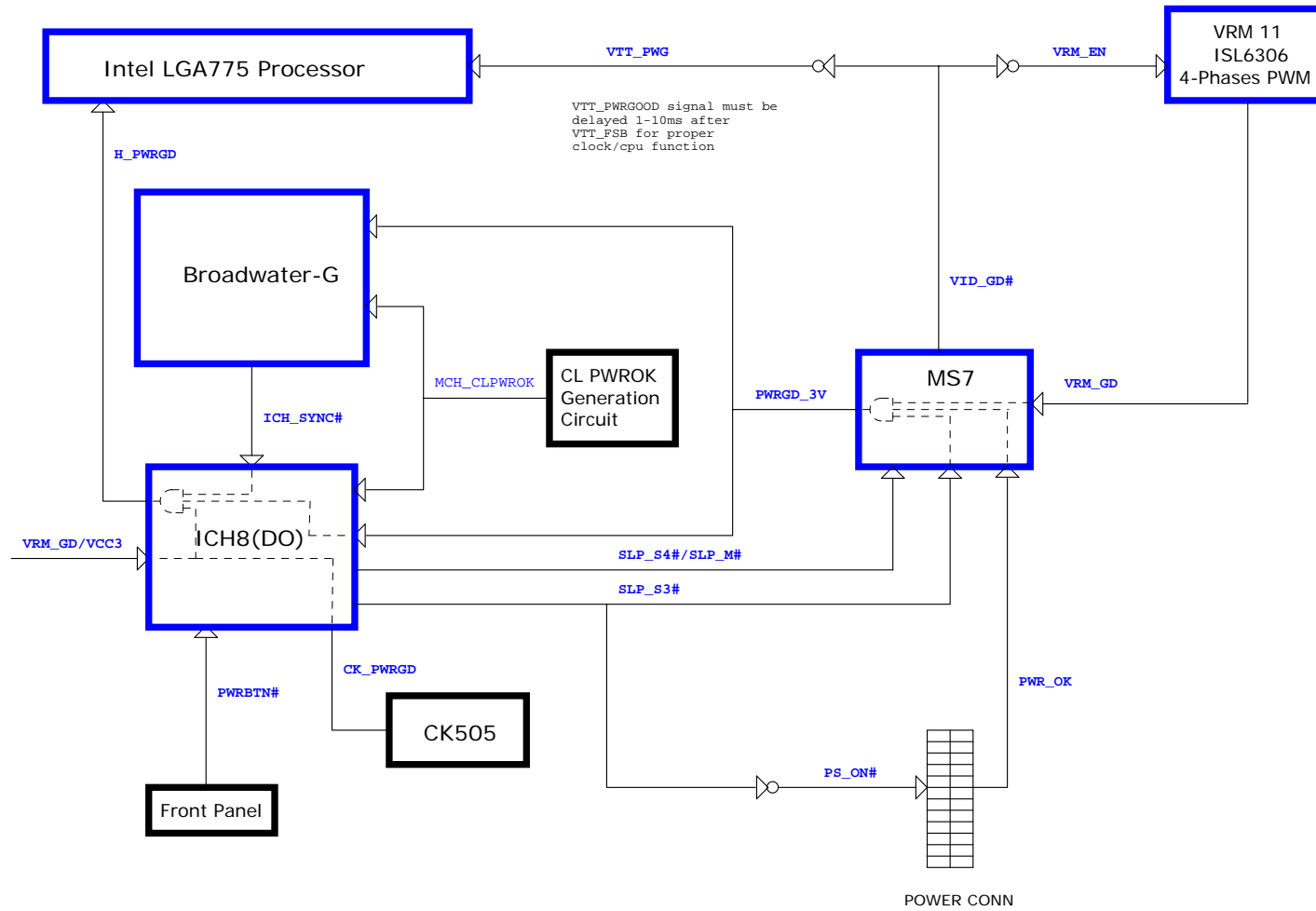
SMBus	Power	Load
SMBCLK	VCC3_SB	ICH8, SIO,PCI EXPRESS x16,x1
SMBCLK_ISO	VCC3	DIMM, CLK GEN, SIO, MS7,LAN

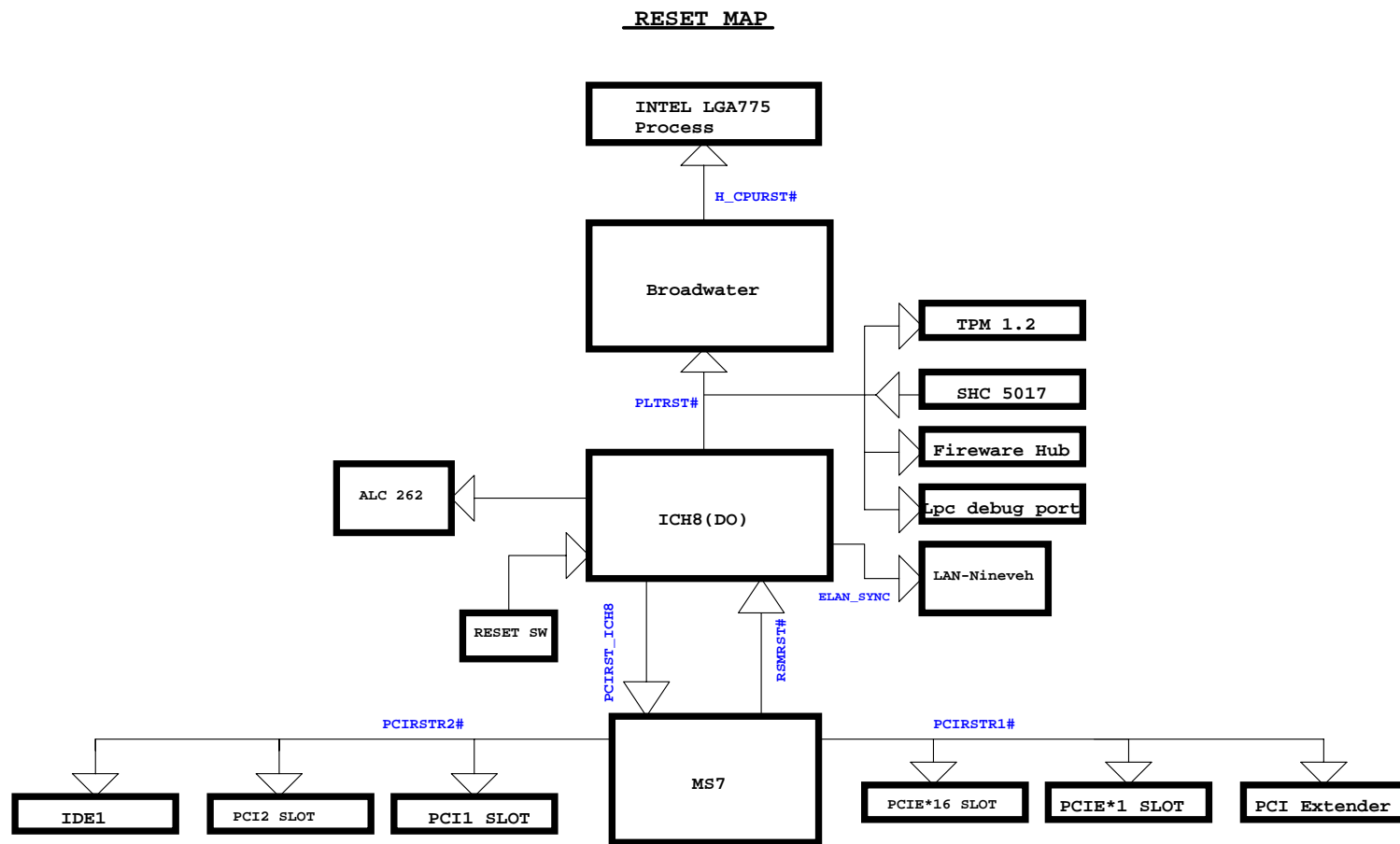
JUMPER SETTING

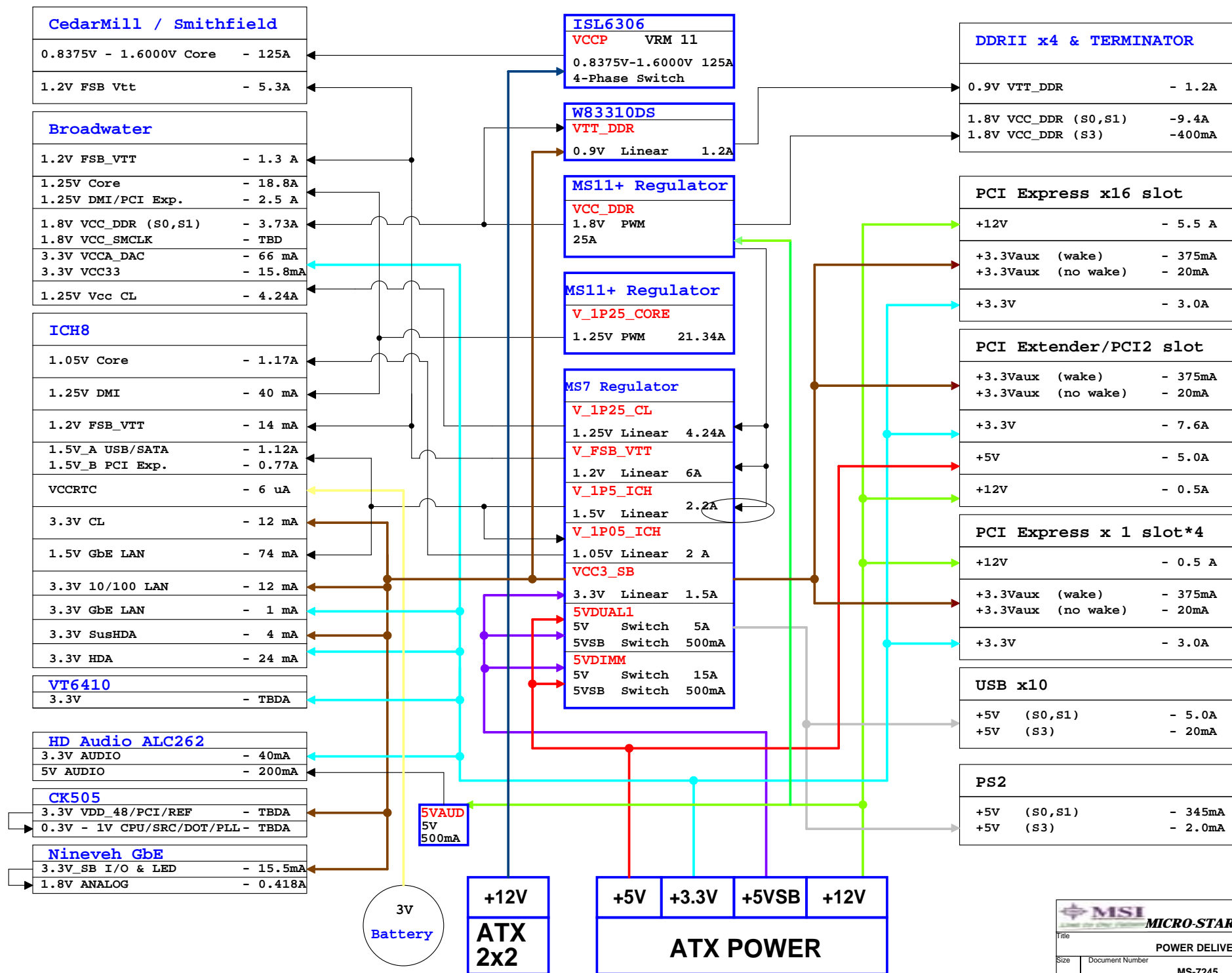
JBAT1	(1-2)Normal	(2-3)Clear
INTRUDER	Short Normal	Open warning
JPWD1	(1-2)Clear	Open Normal

 MICRO-START INT'L CO.,LTD.		
Title		
GPIO PIN definition		
Size	Document Number	Rev
	MS-7245	0A
Date:	Thursday, December 01, 2005	Sheet 31 of 35

PWROK MAP







MANUAL PART

